IEE 1711: Applied Signal Processing

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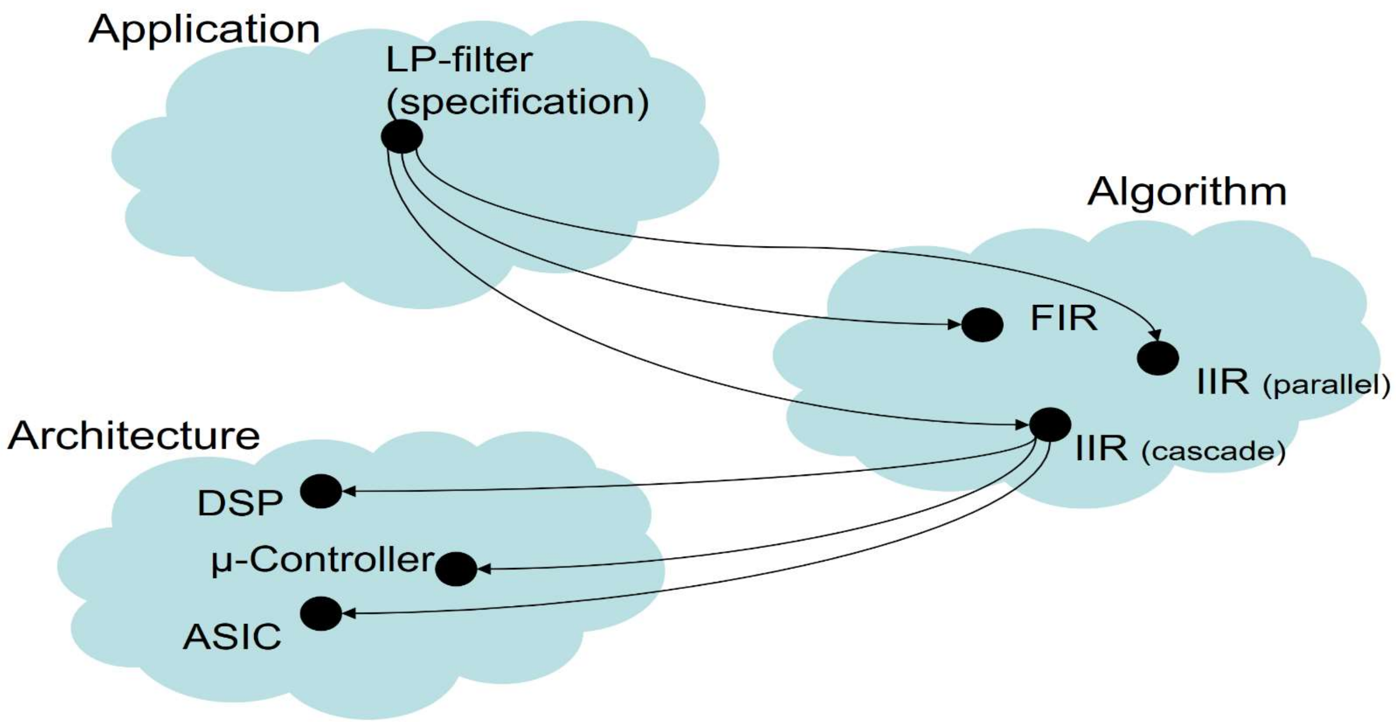
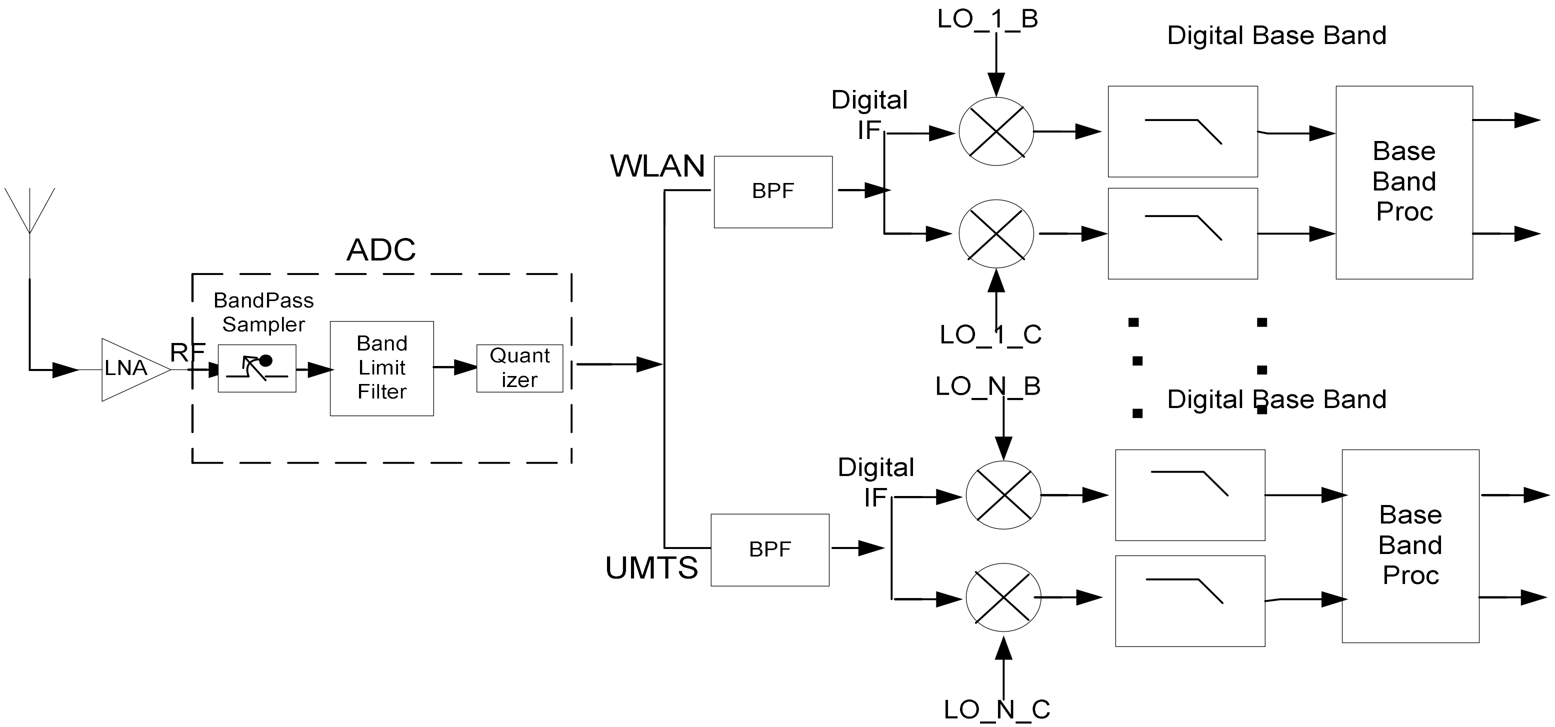


Outline

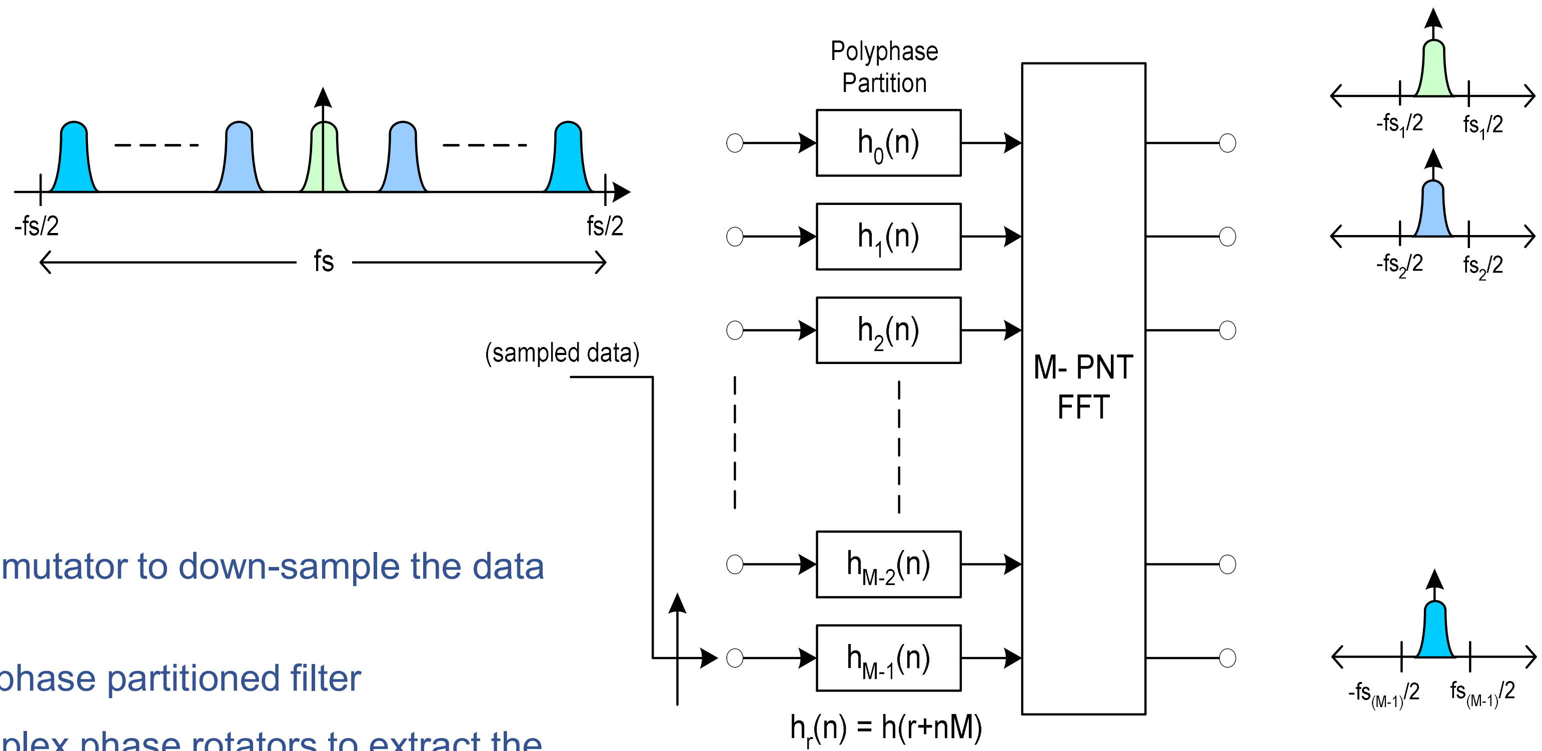
- Recap of MSSRR
- System Design
  - Sampling Frequency Selection
  - Initial Design
  - Constraints
  - Modified Design
  - Optimizations
  - Embedded Re-sampling
- Conclusion

Proposed Software Radio Receiver Architecture

- Digital RF front end
- Digital IF (Decimation & Downconversion)

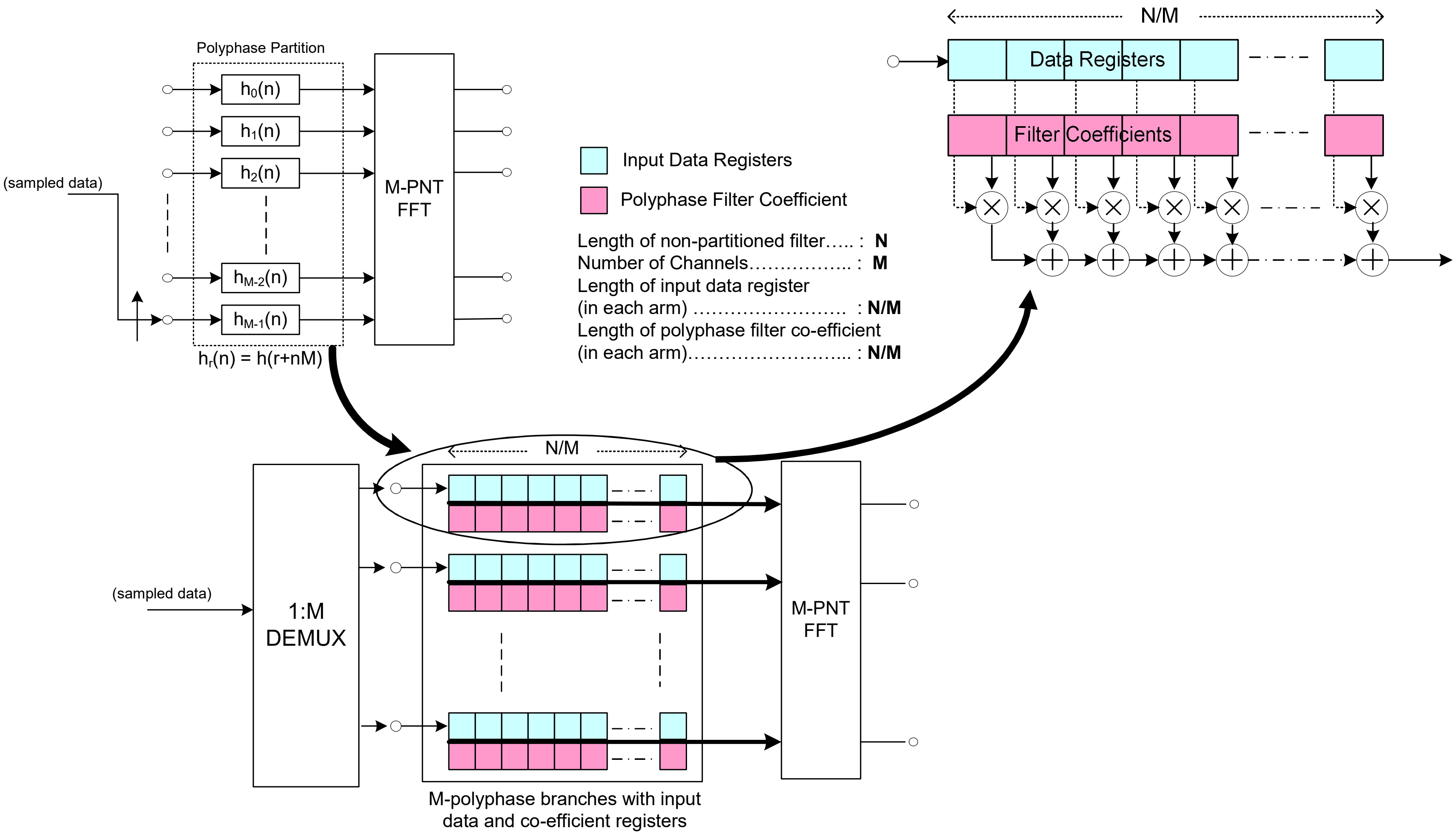


Polyphase channelizer

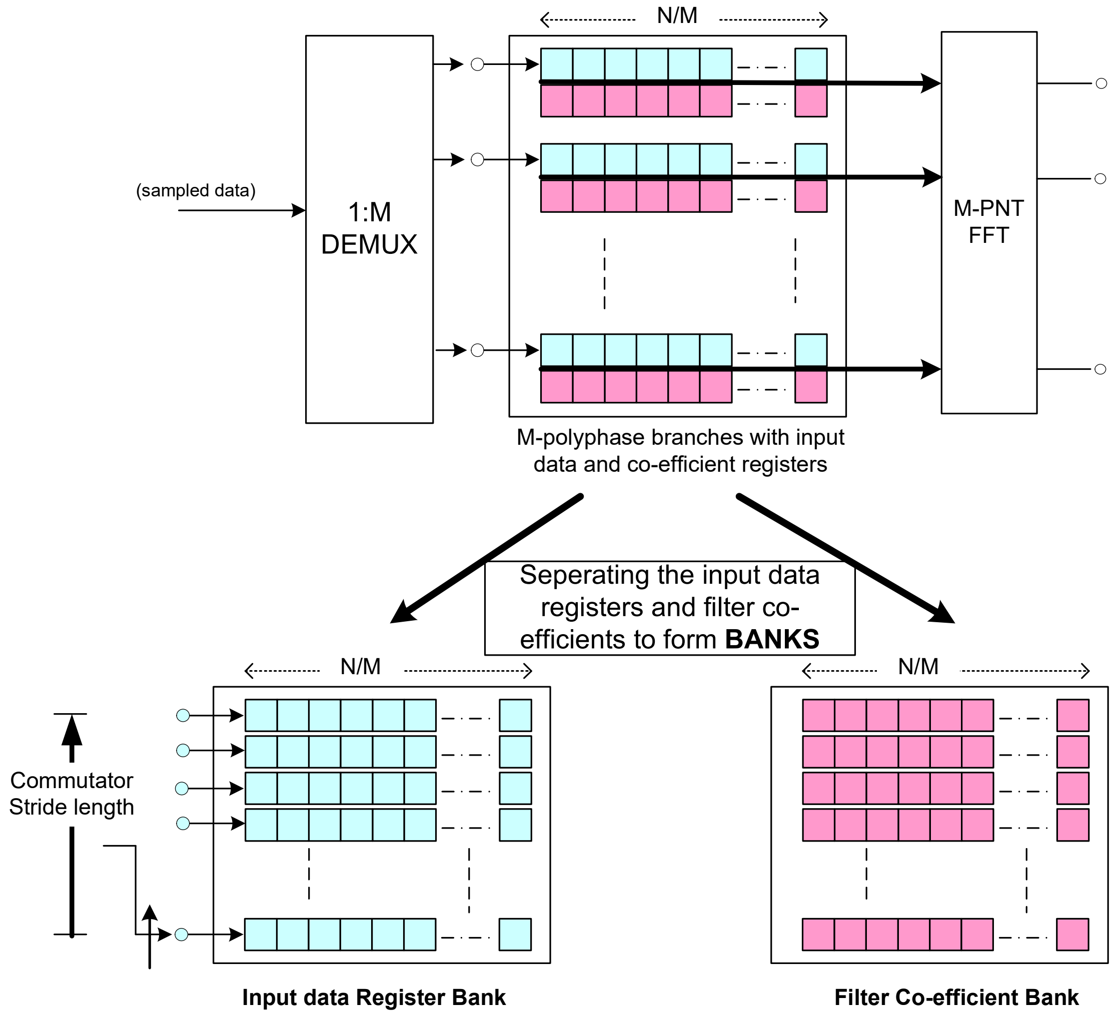


- Commutator to down-sample the data rate
- Polyphase partitioned filter
- Complex phase rotators to extract the individual channels
- Polyphase parameters
  - Input sampling frequency (fs)
  - Inter-carrier spacing (Δf)
  - Number of channels (M)

Polyphase Channelizer Building Blocks



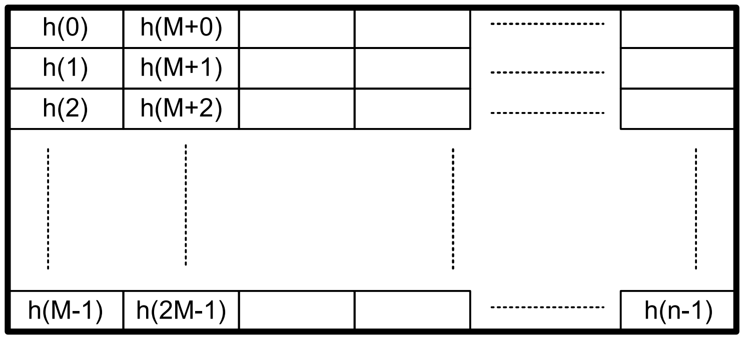
Input Data Reg. & Filter Coeff. Banks

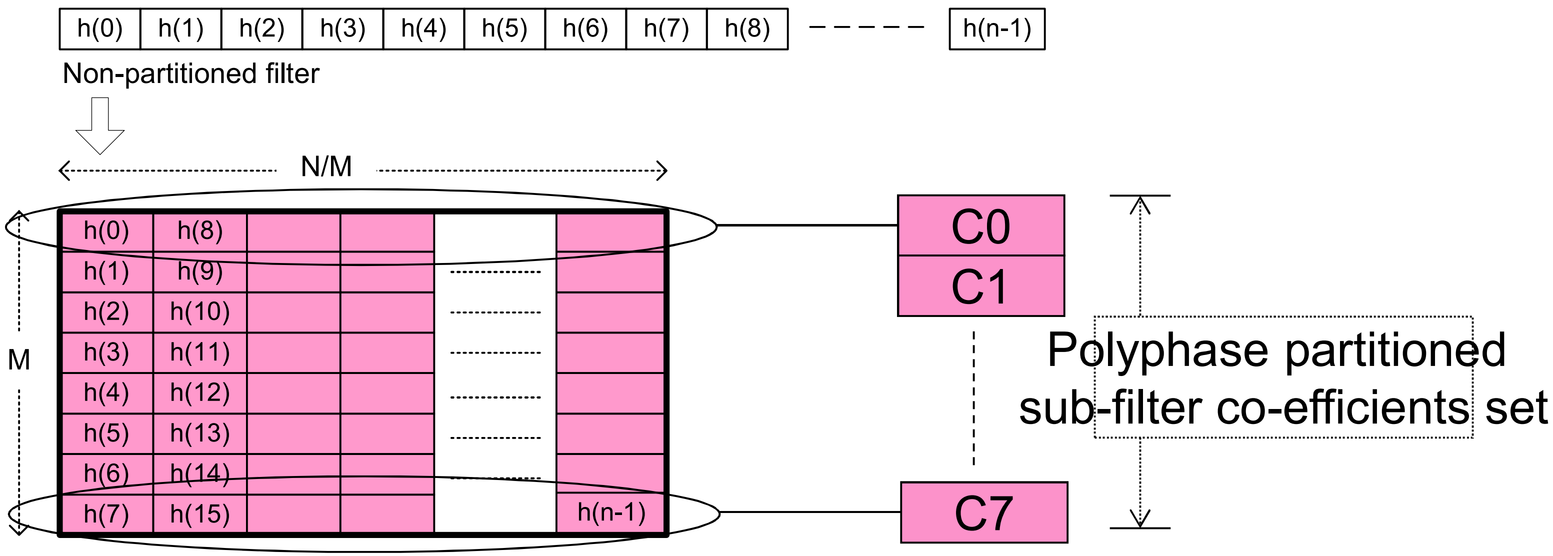


Stride Length:
No. of input samples fed to commutator in order to compute one output sample

Polyphase partitioning

- M-path polyphase partitioning of filter h(n)

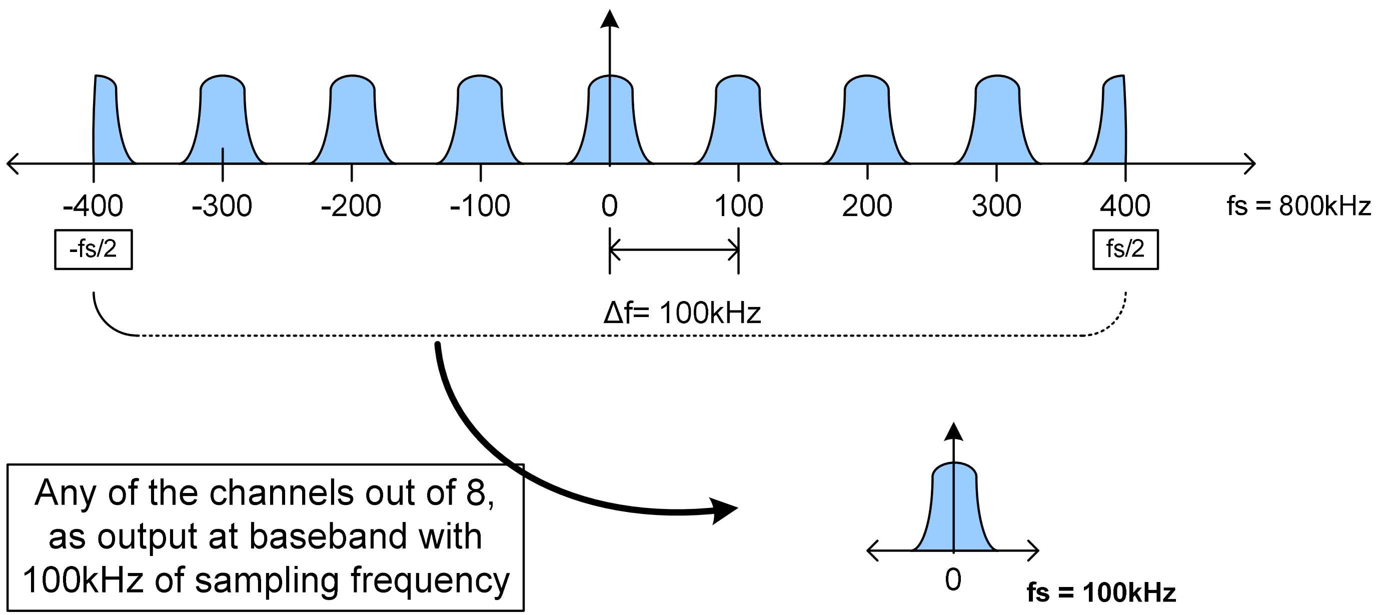




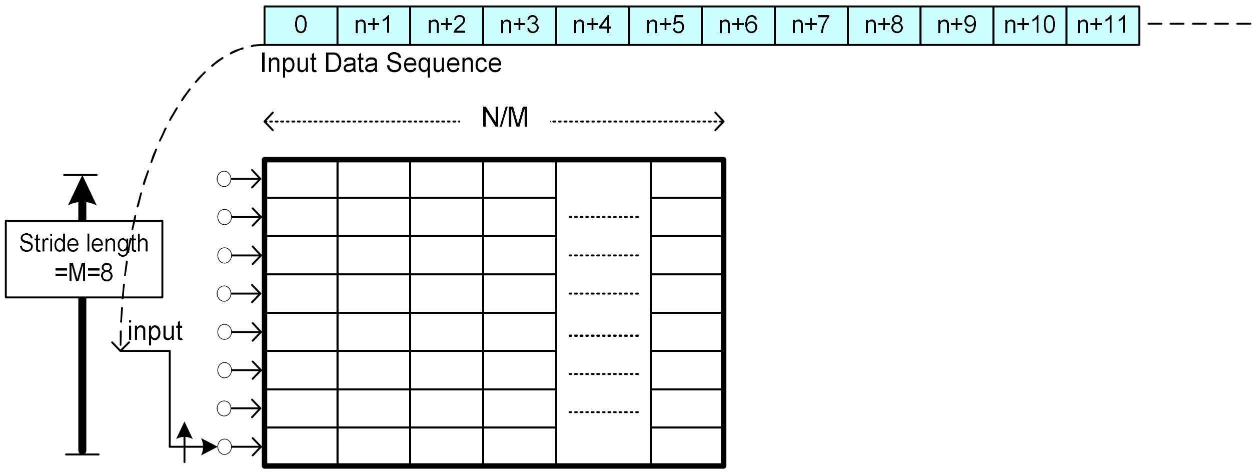
Maximally Decimated System

- **Output sample rate matches the channel spacing (Output $f_s = \Delta f$)**

- Input sampling freq. (f_s): 800kHz
- Inter-channel Spacing (Δf): 100kHz
- $f_s = N . \Delta f$ therefore N=8
- Output sampling rate: 100kHz (**maximally decimated mode**)



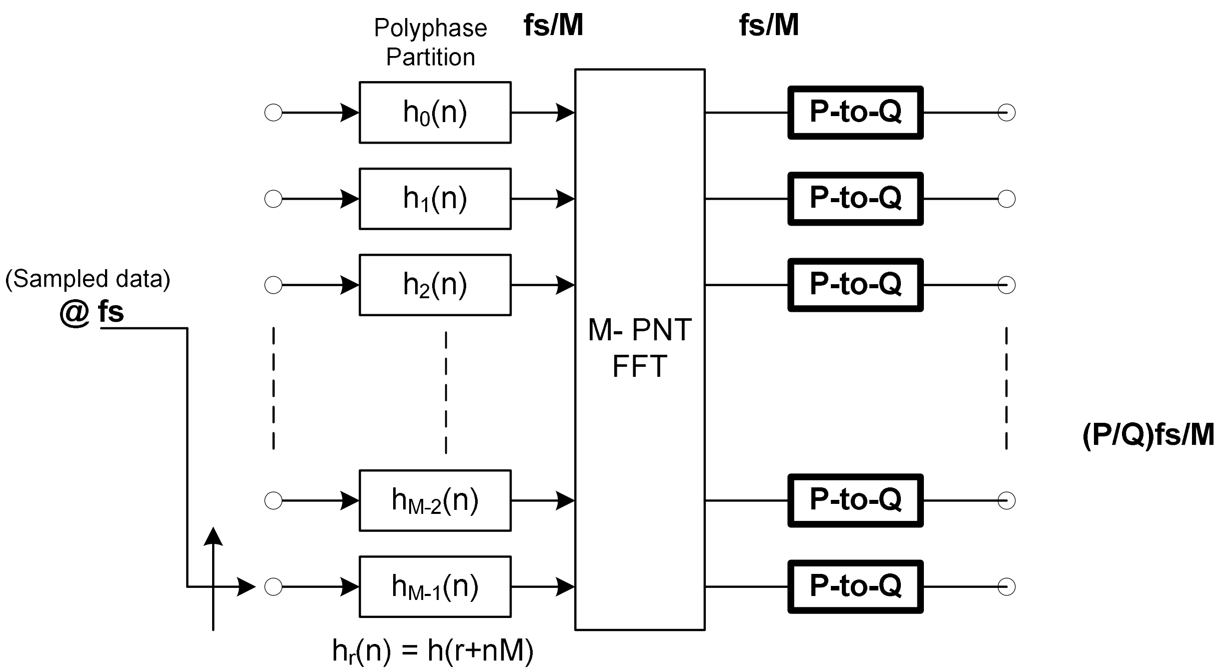
Maximally Decimated System Data Loading Sequence



Input Data Register Bank

Sample-rate changes

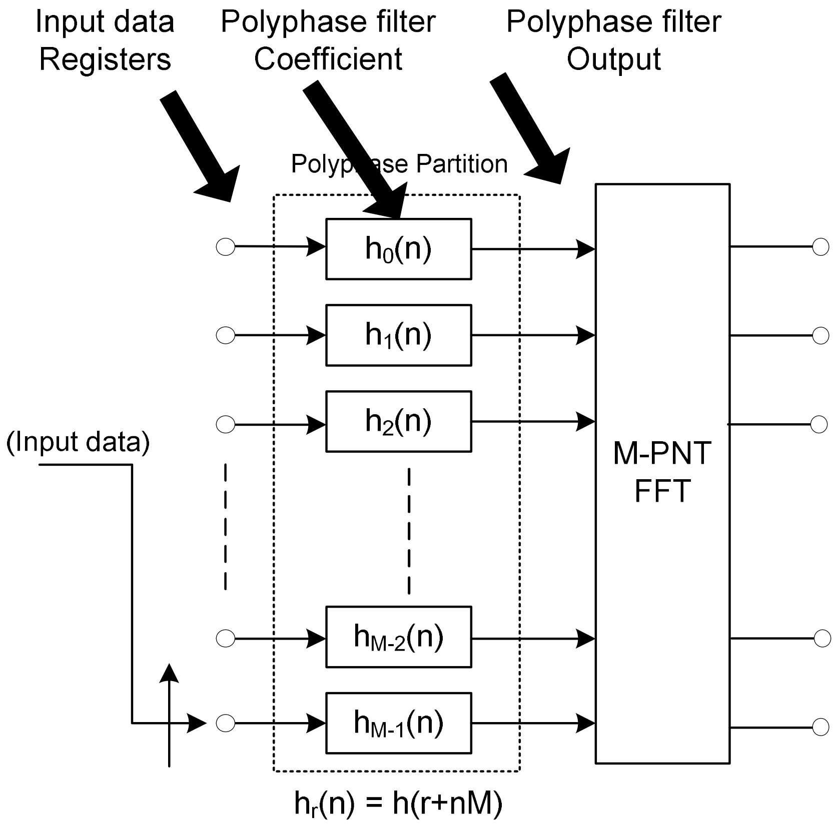
- Straight-forward approach to change the sample rate is after the polyphase channelizer
- By changing the values of P and Q, required sampling rate can be achieved



Alternate Approach (Embedded Re-sampling)

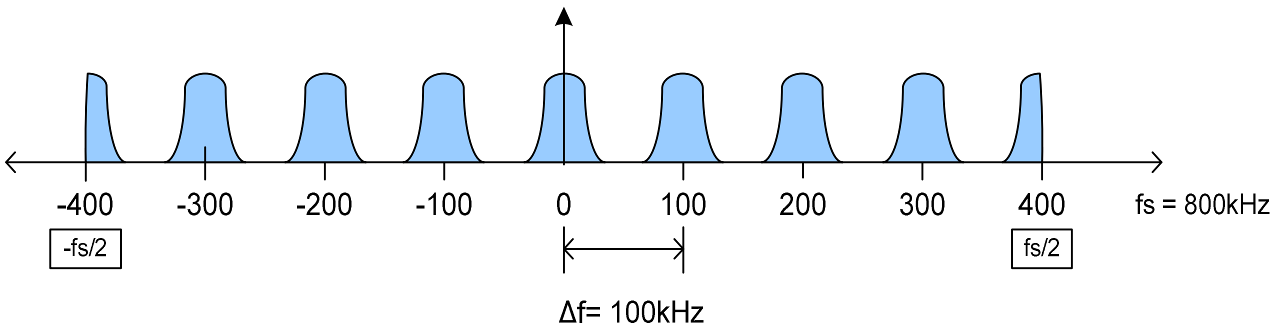
- Embed the re-sampling in the polyphase commutator,
  - in the interaction between input data registers and the polyphase coefficients,
  - and in the interaction between the polyphase outputs and the FFT input

- No computational cost
  - require only a state machine to schedule the interactions



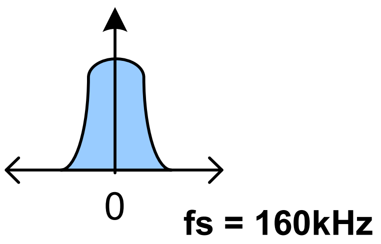
Embedded Re-sampling Examples

- Input sampling freq. (f_s): 800kHz
- Inter-channel Spacing (Δf): 100kHz
- $f_s = N . \Delta f$ therefore N=8
- Output sampling rate: 100kHz (Maximally Decimated Mode)



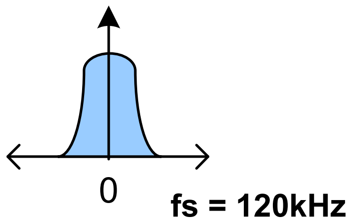
Example #1:

- Required sampling rate: 160kHz (Re-sampling factor: 5)



Example #2:

- Required sampling rate: 120kHz (Re-sampling factor: 20/3)

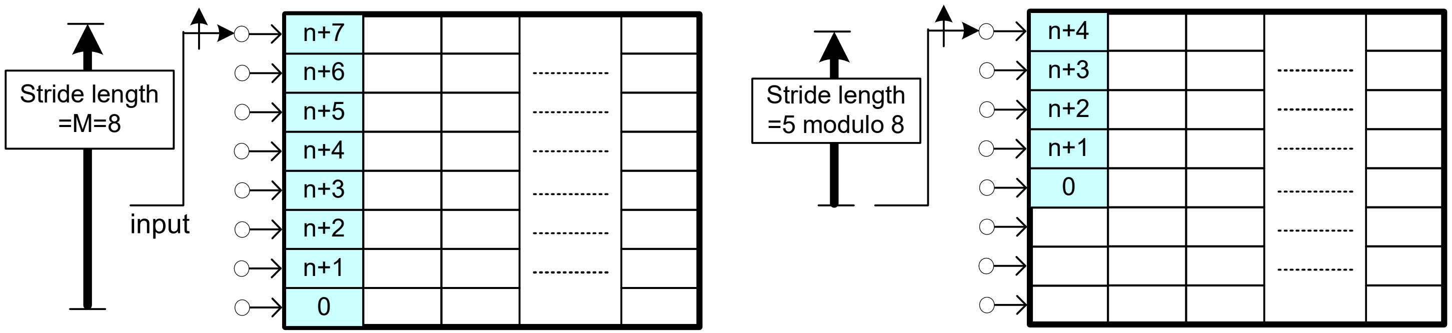


Non-maximally Decimated System
(Down-sampling)

Example #1:

- Input sampling freq. (f_s): 800kHz
- Inter-channel Spacing (Δf): 100kHz
- $f_s = N \cdot \Delta f$ therefore N=8
- **Required sampling rate: 160kHz**
- Modify the input commutator to support 5-1 down-sample rather than 8-1 down sample, keeping the same polyphase paths

> - **Move the data through two dimensional input register memory in stride of length 5 modulo-8.**
> - **Least Common Multiple (LCM) of 5 and 8 is 40, which is the no. of inputs.**
> - **Since 5 inputs are delivered at a time, so there are 8 distinct states in the state machine.**

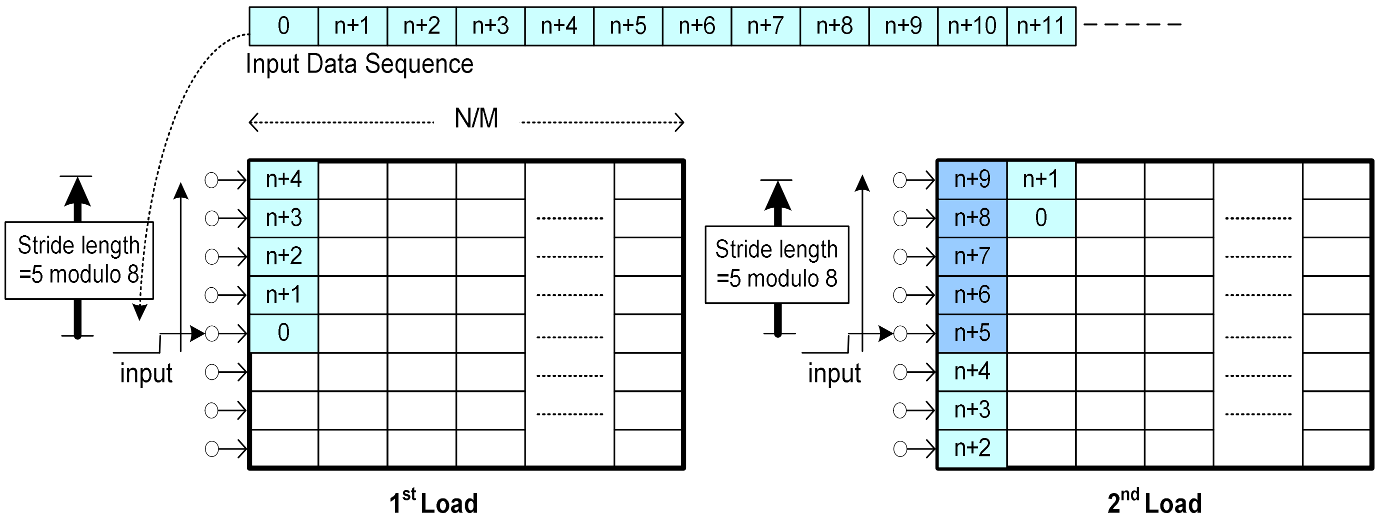


8:1 Down-sampling (Maximally Decimated system)

5:1 Down-sampling (Non-Maximally Decimated system)

Data Loading Operation

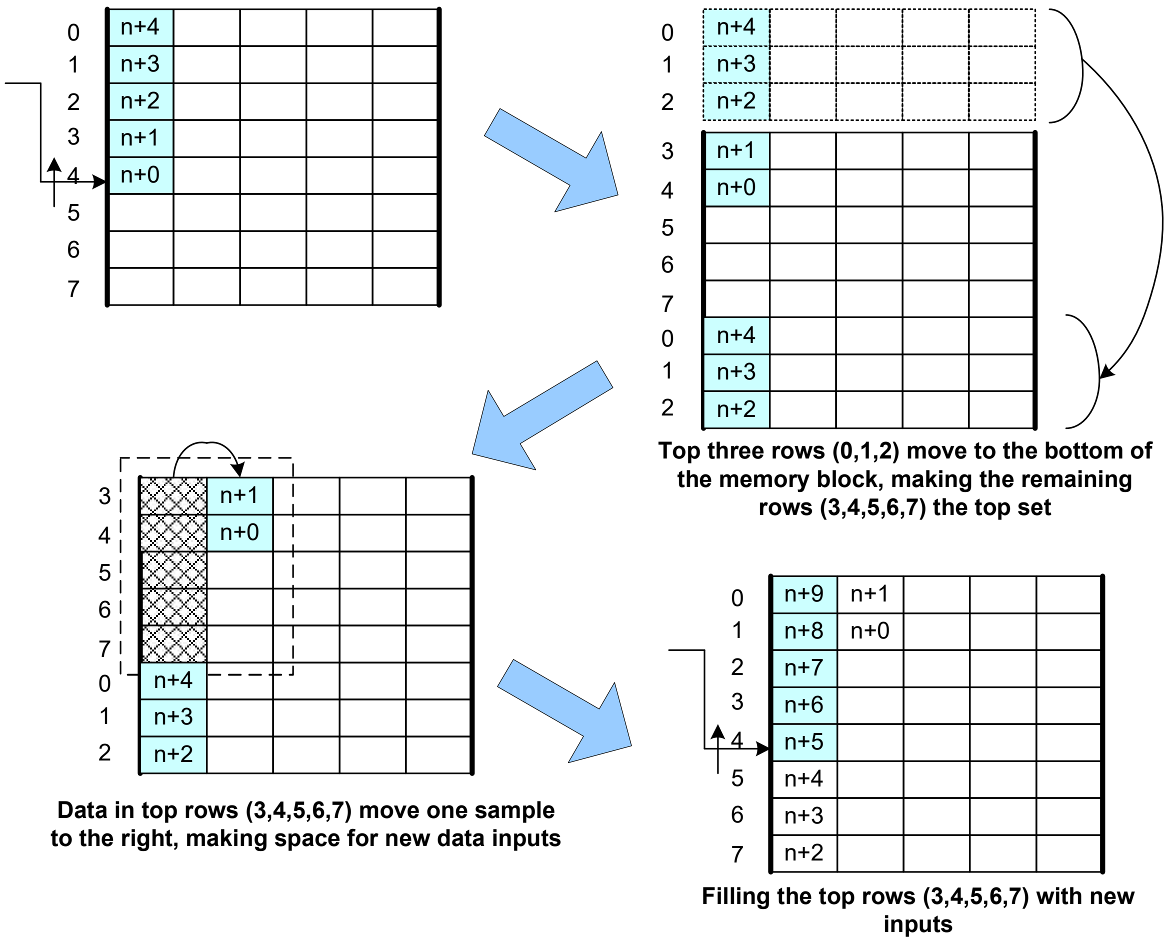
- Polyphase structure can re-sample by any integer factor, 5 in this case.
- Moving all the data in tapped delay line 5 address to the right and loading 5-new inputs before computing the next output.
- Fold the one dimensional tapped delay line into the two dimensional memory of the polyphase filter, then data shifts as **serpentine shift b/w columns**.
- Data loads as the commutator delivering data to the first 5-registers of the left most column.



Successive serpentine data shift in polyphase memory and data load of 5-new inputs for an 8-stage polyphase filter

Serpentine Data Shift

- Data does not actually move by the serpentine shift but rather by circular wrapping of block memory, an address control task
- Filter coefficients are not moved from their original polyphase partition



8-Distinct data feeding states

Stride length =5 modulo-8

Input Data

Residue

n+4				
n+3				
n+2				
n+1				
n+0				

State-0 (Residue =3)

n+9	n+1			
n+8	0			
n+7				
n+6				
n+5				
n+4				
n+3				
n+2				

State-1 (Residue=6)

n+14	n+6			
n+13	n+5			
n+12	n+4			
n+11	n+3			
n+10	n+2			
n+9	n+1			
n+8	0			
n+7				

State-2 (Residue=1)

n+19	n+11	n+3		
n+18	n+10	n+2		
n+17	n+9	n+1		
n+16	n+8	n+0		
n+15	n+7			
n+14	n+6			
n+13	n+5			
n+12	n+4			

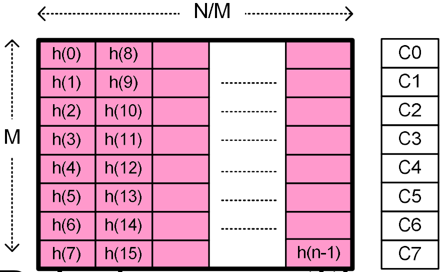
State-3 (Residue=4)

n+24	n+16	n+8	0	
n+23	n+15	n+7		
n+22	n+14	n+6		
n+21	n+13	n+5		
n+20	n+12	n+4		
n+19	n+11	n+3		
n+18	n+10	n+2		
n+17	n+9	n+1		

State-4 (Residue=7)

n+29	n+21	n+13	n+5	
n+28	n+20	n+12	n+4	
n+27	n+19	n+11	n+3	
n+26	n+18	n+10	n+2	
n+25	n+17	n+9	n+1	
n+24	n+16	n+8	n+0	
n+23	n+15	n+7		
n+22	n+14	n+6		

State-5 (Residue=2)



Polyphase partitioned Sub-filter co-efficient sets, are same for all states

n+34	n+26	n+18	n+10	n+2
n+33	n+25	n+17	n+9	n+1
n+32	n+24	n+16	n+8	0
n+31	n+23	n+15	n+7	
n+30	n+22	n+14	n+6	
n+29	n+21	n+13	n+5	
n+28	n+20	n+12	n+4	
n+27	n+19	n+11	n+3	

State-6 (Residue-5)

n+39	n+31	n+23	n+15	n+7
n+38	n+30	n+22	n+14	n+6
n+37	n+29	n+21	n+13	n+5
n+36	n+28	n+20	n+12	n+4
n+35	n+27	n+19	n+11	n+3
n+34	n+26	n+18	n+10	n+2
n+33	n+25	n+17	n+9	n+1
n+32	n+24	n+16	n+8	0

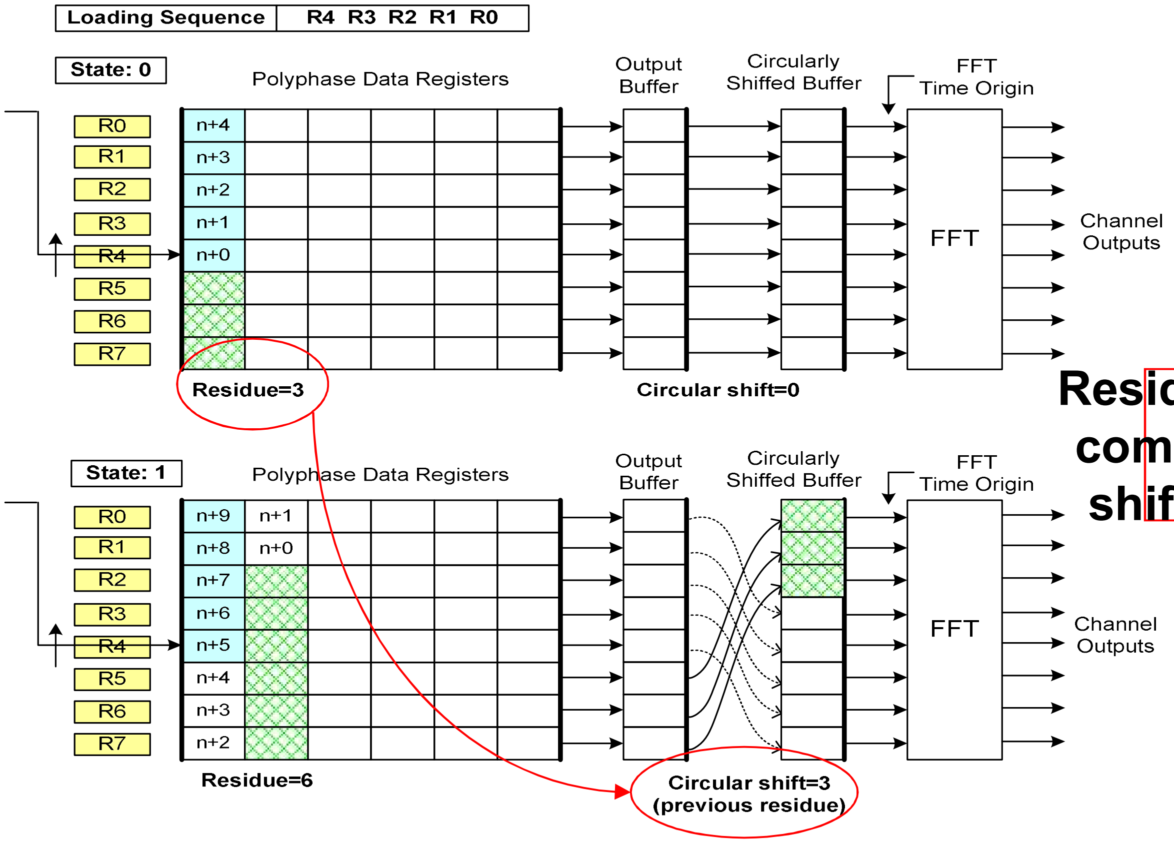
State-7 (Residue=0)

n+44	n+36	n+28	n+20	n+12	n+4
n+43	n+35	n+27	n+19	n+11	n+3
n+42	n+34	n+26	n+18	n+10	n+2
n+41	n+33	n+25	n+17	n+9	n+1
n+40	n+32	n+24	n+16	n+8	0
n+39	n+31	n+23	n+15	n+7	
n+38	n+30	n+22	n+14	n+6	
n+37	n+29	n+21	n+13	n+5	

State same as **State-0**

- Move the data through two dimensional input register memory in stride of length 5 modulo-8.
- Least Common Multiple (LCM) of 5 and 8 is 40, which is the no. of inputs.
- Since 5 inputs are delivered at a time, so there are 8 distinct states in the state machine.

Serpentine shifting & Circular Buffering

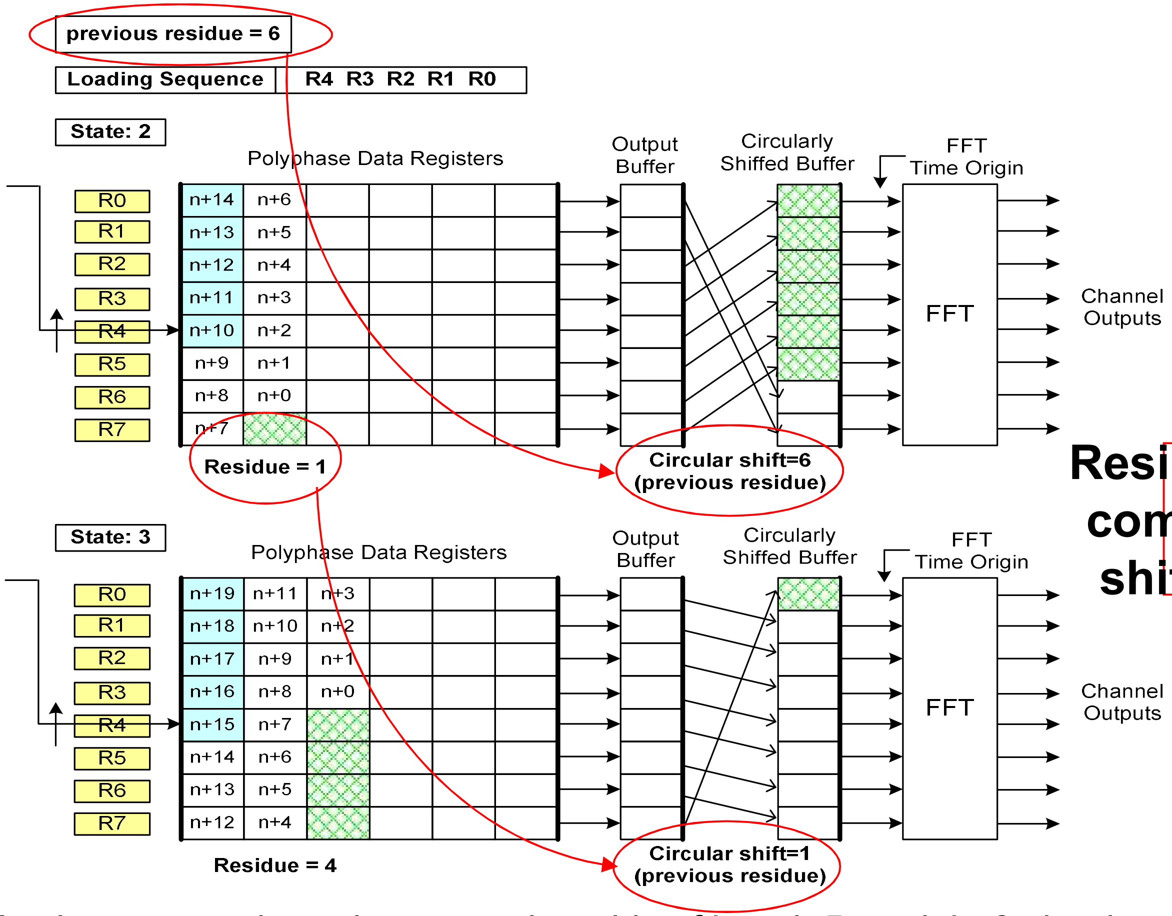


Residue in current state is compensated by circular shifting in the next state

- As data moves through memory in-stride of length 5-modulo-8, the data time origin precesses w.r.t FFT time origin

- The two origins are aligned by circularly shifting the computed outputs of the polyphase filter by the residue address of the data time origin modulo-8

Serpentine shifting & Circular Buffering ….



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- The two origins are aligned by circularly shifting the computed outputs of the polyphase filter by the residue address of the data time origin modulo-8

Results

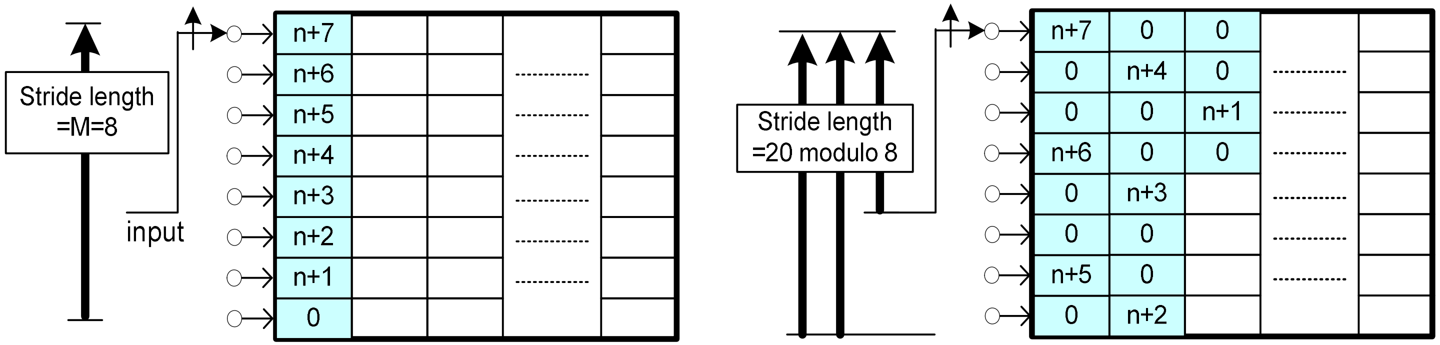
- Polyphase structure can re-sample by any integer factor.
- The commutator interacting with the polyphase filter determines the output sample rate.
- In serpentine shifting and circular buffering scheme:
  - the input data is fed to same registers all the time.
  - Input data registers are serpentine shifted before loading new data
  - Polyphase sub-filter co-efficients are fixed to their branches.
  - Output from polyphase filter bank is circularly shifted to undone the time-offset by serpentine shifting before the FFT operation.
- In sliding cyclic load and cyclic shift of the co-efficient memory scheme:
  - the input data is fed as sliding cyclic load by the input commutator to a fixed set of registers
  - Polyphase sub-filter co-efficients are cyclic shifted.
- In similar fashion, a down sample 10:1 in an 8-point polyphase filter can down-convert the same centre frequencies multiples of 100KHz, while maintaining the output sample rate of 800/10 = 80KHz

Non-maximally Decimated System
(Simultaneous Up-sampling & Down-sampling)

Example #2:

- Input sampling freq. (f_s): 800kHz
- Inter-channel Spacing (Δf): 100kHz
- $f_s = N \cdot \Delta f$ therefore N=8
- **Required sampling rate: 120KHz (re-sampling ratio: 20/3)**

- **First up sampling by 3 and then down sampling by 20**
- **Up sampling - zero packing the input data**
- **Down sampling by serpentine shifting data through the filter in stride of length 20.**



8:1 Down-sampling (Maximally Decimated system)

20:1 Down-sampling (Non-Maximally Decimated system)

Serpentine Shifting the data

- In first load, 7-actual data samples are delivered to the 20 registers addresses.
- In 2nd load, 6-actual data samples are delivered to the 20 registers addresses.
- The loading sequence is found to be periodic in **6 cycles**, which requires 6 states machines.
- No zero-packing in the final configuration.

Input Data →

n+1	n+**2**	n+3	n+4	n+**5**	n+6	n+7	n+8	– – – – –

Zero-packed Data (Up-sampled 1:3) →

0	n+1	0	0	n+**2**	0	0	n+3	0	0	n+4	– – – – –

1^{st} Load

n+7	0	0		
0	n+4	0		
0	0	n+1		
n+6	0	0		
0	n+3			
0	0			
n+5	0			
0	n+2			

2^{nd} Load

0	n+11	0	0	n+3
0	0	n+8	0	0
n+13	0	0	n+5	0
0	n+10	0	0	n+2
0	0	n+7	0	0
n+12	0	0	n+4	0
0	n+9	0	0	n+1
0	0	n+6	0	0

Successive serpentine data shift in polyphase memory and data load for a 20/3 re-sampling in an 8-stage polyphase filter

- **Move the data (zero-packed) through two dimensional input register memory in stride of length 20.**
- **Least Common Multiple (LCM) of 20 and 8 is 40, which is total no. of inputs.**
- **Since 20 (zero-packed) inputs are delivered at a time, so it requires 2 cycles**
- **For up-sampling factor of 3, LCM of 2 and 3 is 6, which is the periodic interval for state machines.**

Polyphase Filter Bank Parameters

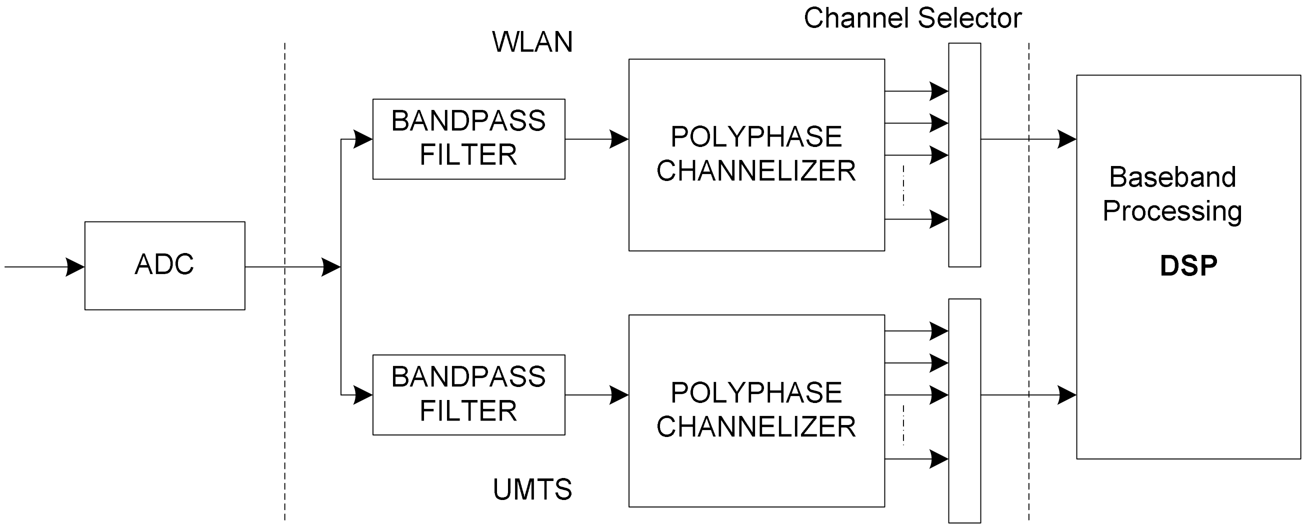
Sampling Frequency, Number of Channels, Spectral Spacing, Output Sample Rate.

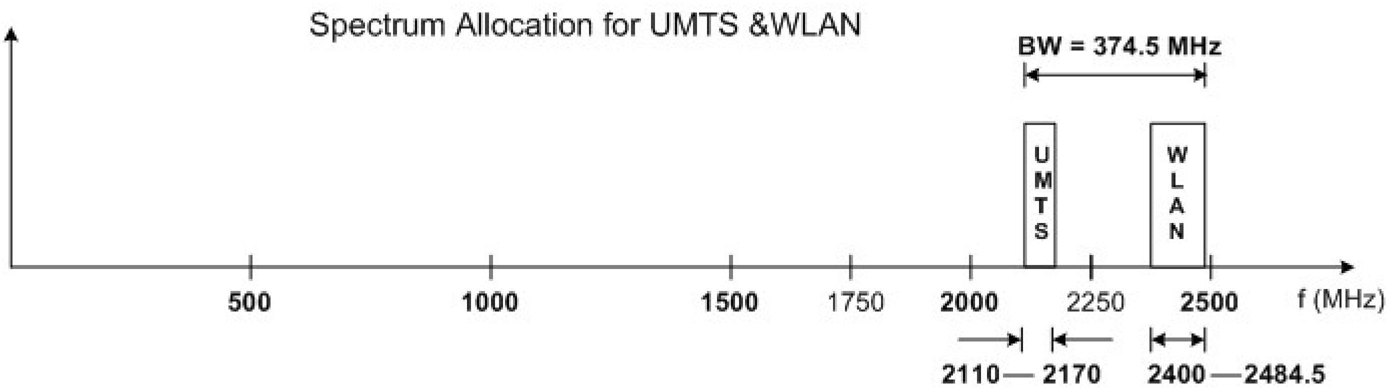
$$fs = N * \Delta f$$

- DFT performs the task of seperating the channels after polyphase filter, so it is natural to conclude that **transform size is equal to number of channels.**
- **The filter bandwidth is determined by the weights of the low pass prototype filter, and it is common for all the channels.**
- Channelizer is used to seperate the adjacent communication channels, which are characterized by the **specifc center frequency and non-overlapping bandwidth**

WLAN & UMTS Channelizers

System Level Diagram

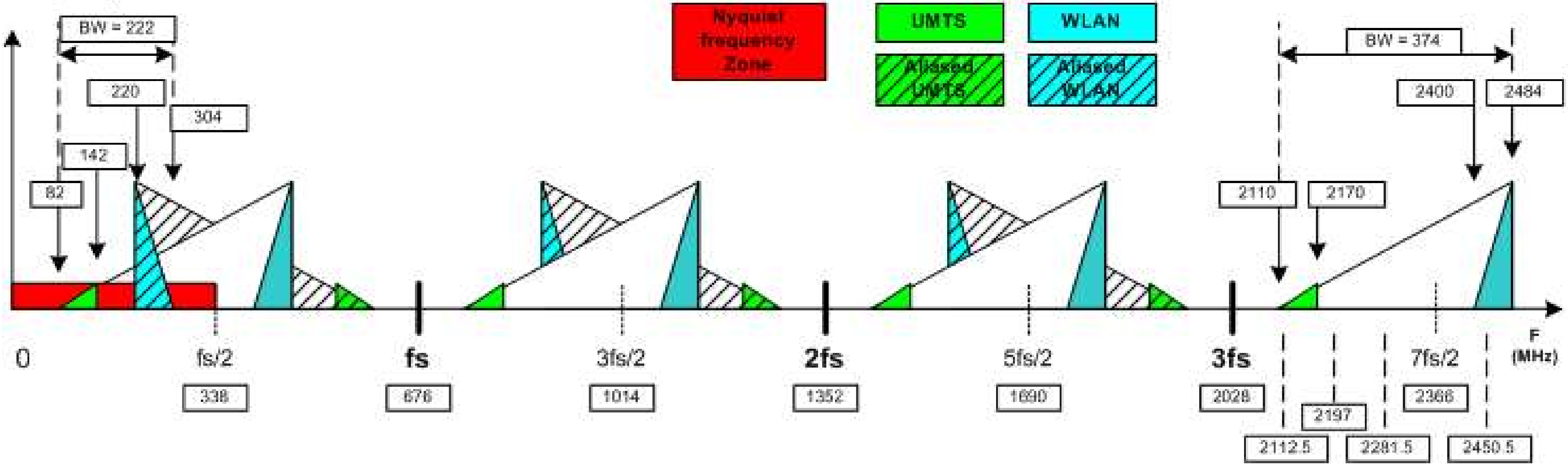




Selection of Sampling Frequency

- **Combined band (373.5MHz) of UMT & WLAN requires at least 747MHz of sampling frequency (Bandpass sampling) to have non-overlap aliases**
- **Sampling freq. of 676MHz results in overlap aliases but UMTS &WLAN channels are still non-overlapped**

Bandpass Sampling : A band including multi-standards (UMTS & WLAN) is undersampled @ 676 MHz and the Nyquist frequency band (0-338MHz) contains the aliases of the standard signals. The aliases of the receiving band are overlapped but aliases for individual standard bands are still non-overlapped. The WLAN becomes spectrally inverted in the Nquist frequncy zone.



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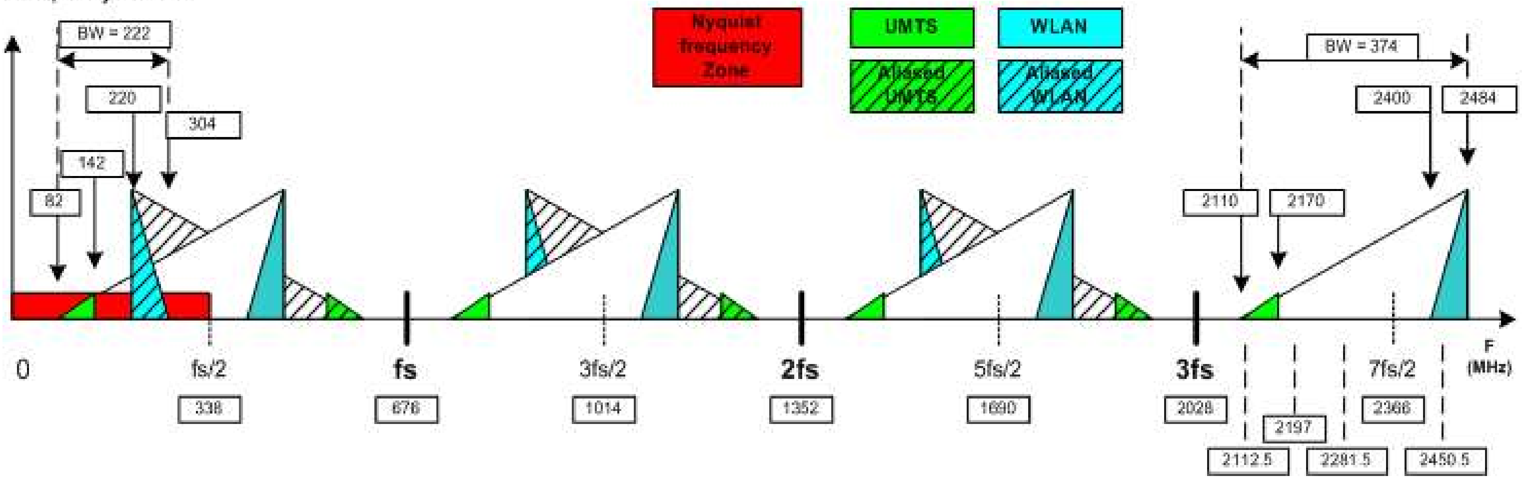
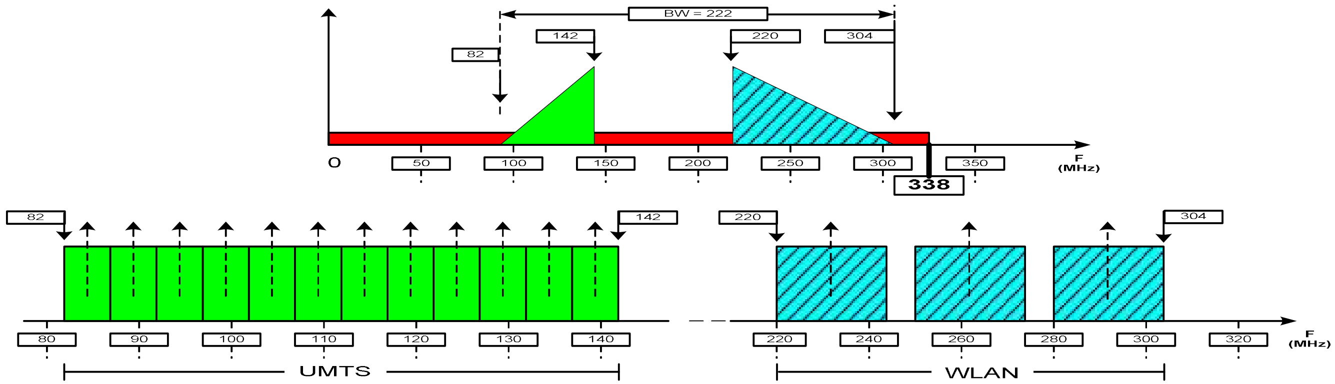
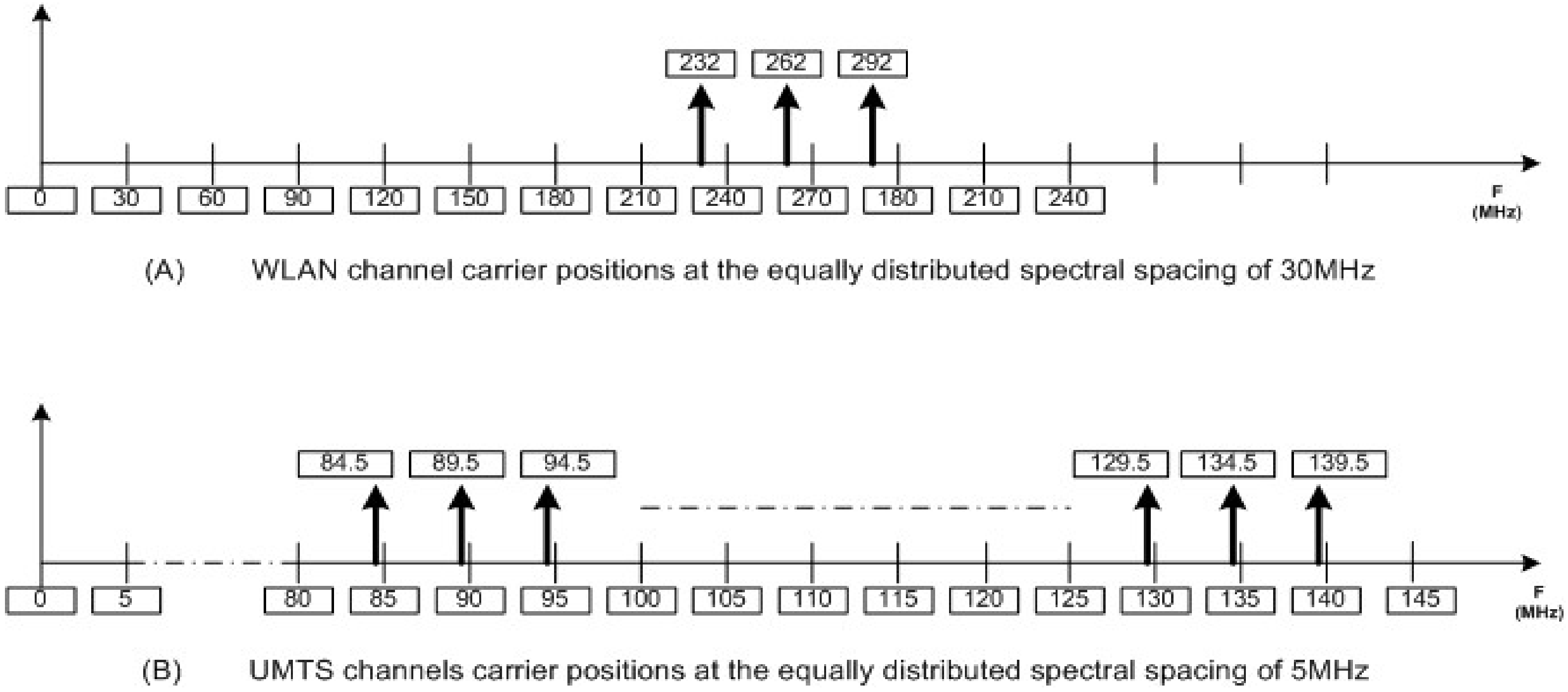


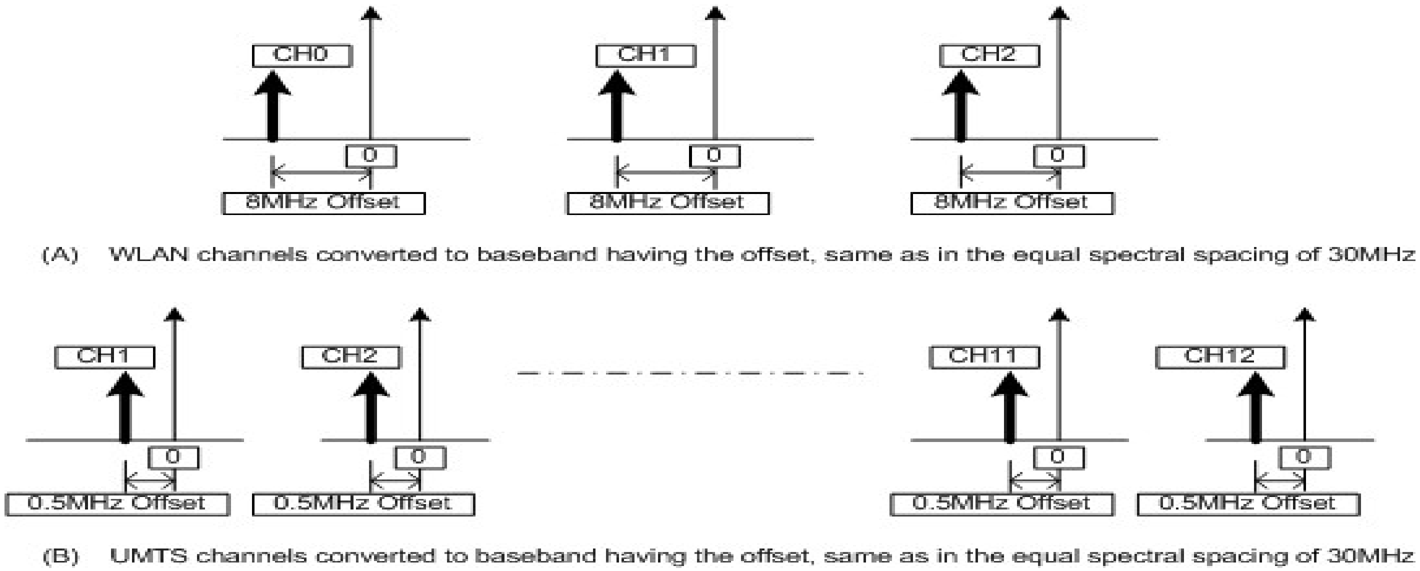


Spectral Distribution of WLAN & UMTS Channels



Equal spectral distribution of WLAN and UMTS spectrum to 30 and 5MHz channel spacing respectively. Non of the WLAN and UMTS channels become centered on the multiples of 30 and 5 MHz placing respectively.

Channelization results in corresponding offset from the baseband



Channelization results in corresponding offset from the baseband for each of the converted channel, due to non-centered channels on the equally distributed spectral placing.

Polyphase channelizer for UMTS and WLAN

UMTS

- Input sampling freq. (fs): 676MHz
- Inter-channel Spacing (Δf): 5MHz
- Number of Channels (N)
- fs = N . Δf

  therefore **N=135.2**

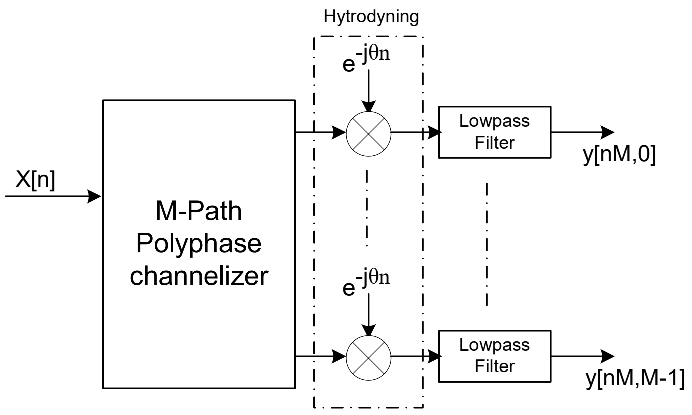
WLAN

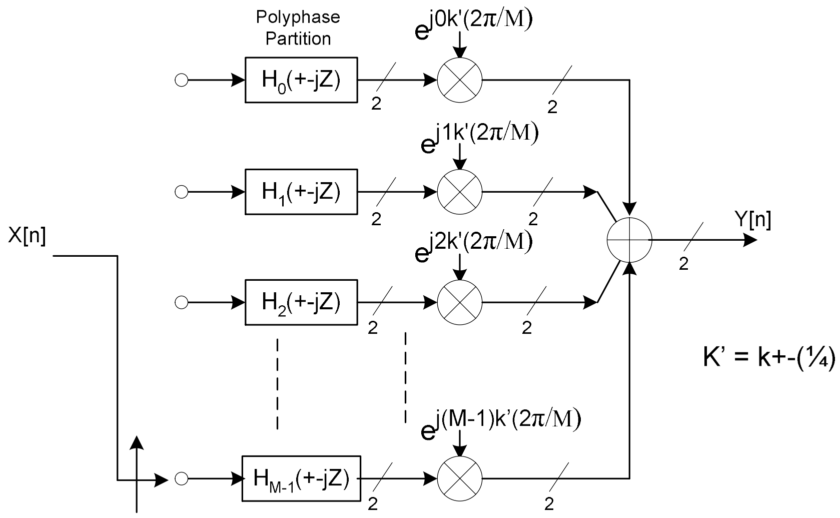
- Input sampling freq. (fs): 676MHz
- Inter-channel Spacing (Δf): 30MHz
- Number of Channels (N)
- fs = N . Δf

  therefore **N=22.53**

- Resulted channels do not fulfil polyphase channelizer requirements
- fs and Δf can be changed to have integer no. of channels
- Violation of second requirement results in offset of the down-converted channels from the baseband
  - Change the sampling frequency so that the resulted aliased channels lie on equal spectral placing
  - Heterodyne the offset channels to have them at baseband
  - Embed the Heterodyning in the polyphase structure

Compensating Baseband Offset





Polyphase Filter Bank
with +-j Rotators

- Hyterodyning to compensate the offset of the baseband channels
- It requires a separate Hyterodyning at each of the channels
- The required mixer can be restricted to +-1 or 0 if the required hyterodyne is a simple translation from the quarter sampling rate to the base band (results in no actual multiplication)

- Hyterodyning is embedded in the polyphase structure
- Best for offsets of the quarter multiples of the channels spacing
- Filter coefficients are pre-rotated before loading to filter banks
- Offset is also embedded in the polyphase rotator on each polyphase arm

Channelizer based on Variant Polyphase Structure

WLAN

- Baseband offsets of 8MHz : not the quarter sub-multiple of channel spacing of 30MHz

UMTS

- Baseband offsets of 0.5MHz : not the quarter sub-multiple of channel spacing of 5MHz.

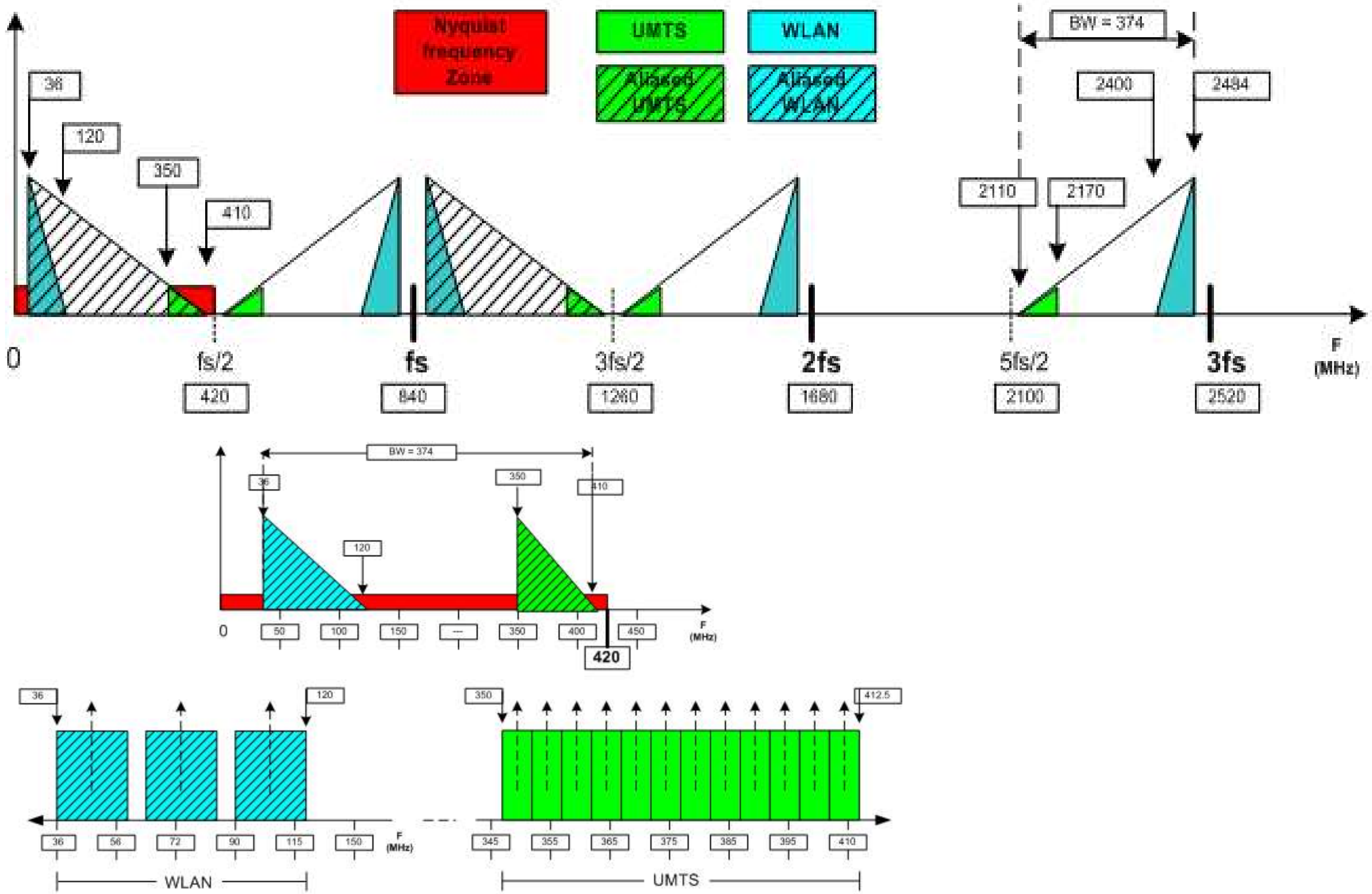
Two solutions:

- Resample the input data fed to the channelizers
  - Different re-sampling factors can be tried to solve the problem

- Change the sampling frequency of the system (other than 676MHz)
  - Different sampling frequencies are tried and finally 840MHz is selected (that meets the polyphase channelizer requirements)

Bandpass Sampling @ 840MHz

Bandpass Sampling : A band including multi-standards (UMTS & WLAN) is undersampled @ 840 MHz and the Nyquist frequency band (0-420MHz) contains the aliases of the standard signals. The aliases of the combined band of 374MHz are non-overlapped. The WLAN and UMTS both are spectrally inverted in the Nquist frequncy zone.



Modified Channelizers

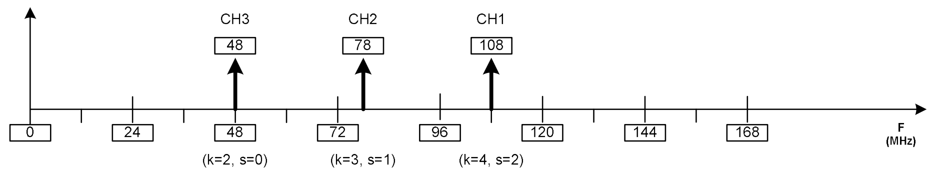
- Input sampling freq. (f_s): 840MHz

WALN

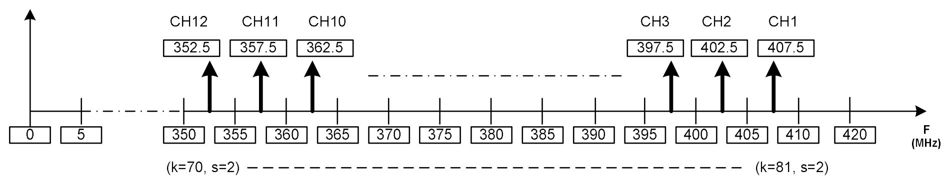
- Inter-channel Spacing (Δf): 24MHz
- $f_s = N . \Delta f$ therefore N=35

UMTS

- Inter-channel Spacing (Δf): 5MHz
- $f_s = N . \Delta f$ therefore N=168

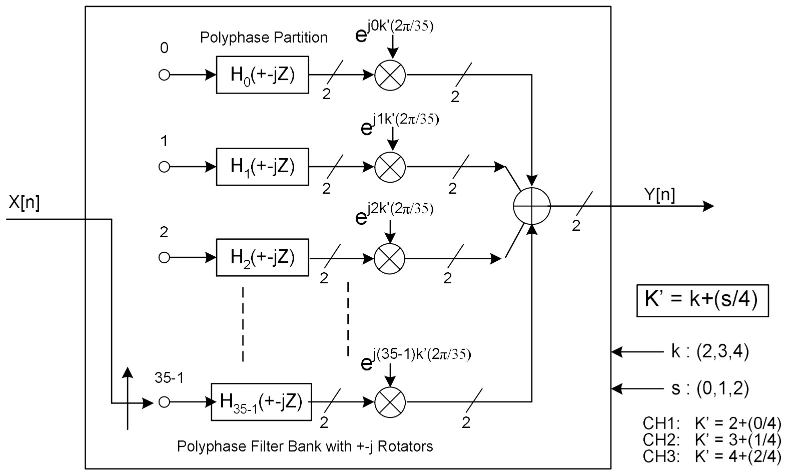


(A) WLAN channel carrier positions at the equally distributed spectral spacing of 24MHz



(B) UMTS channels carrier positions at the equally distributed spectral spacing of 5MHz

Polyphase Channelizer for WLAN



Polyphase Channelizer for UMTS