IEE 1711: Applied Signal Processing

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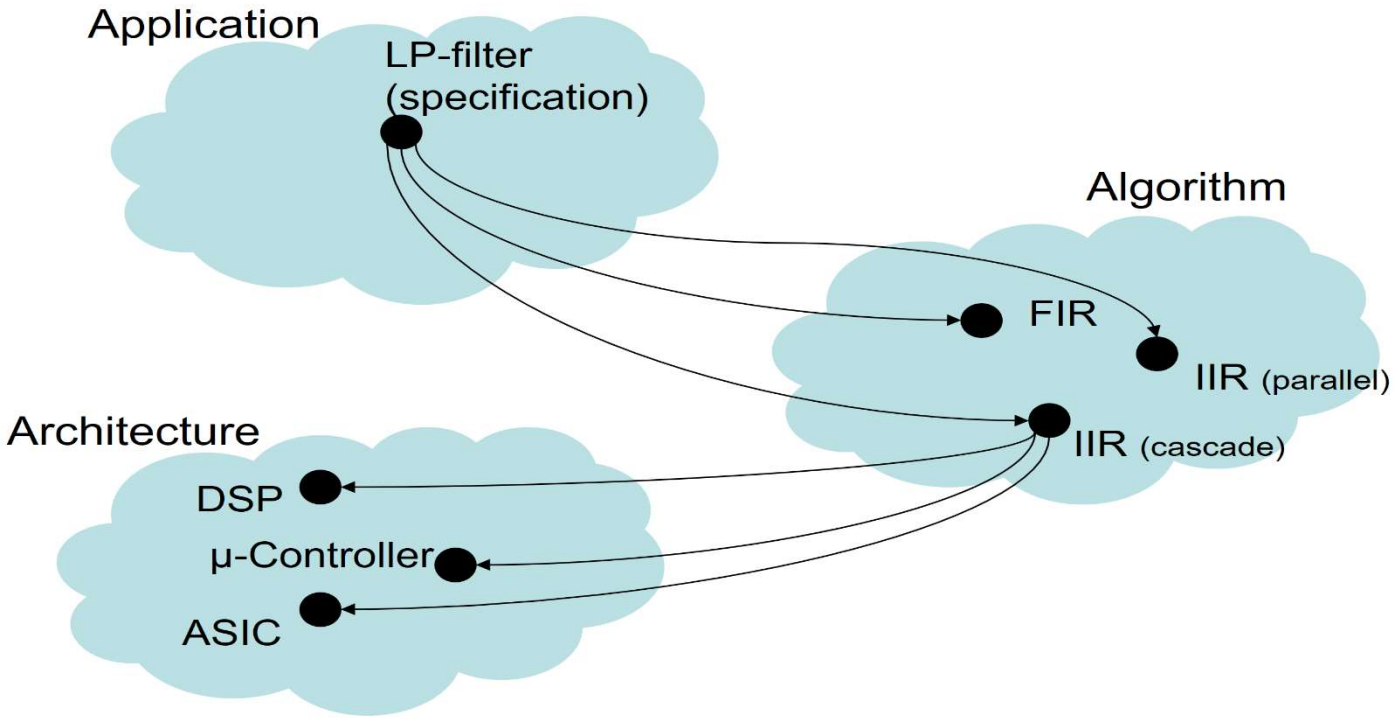


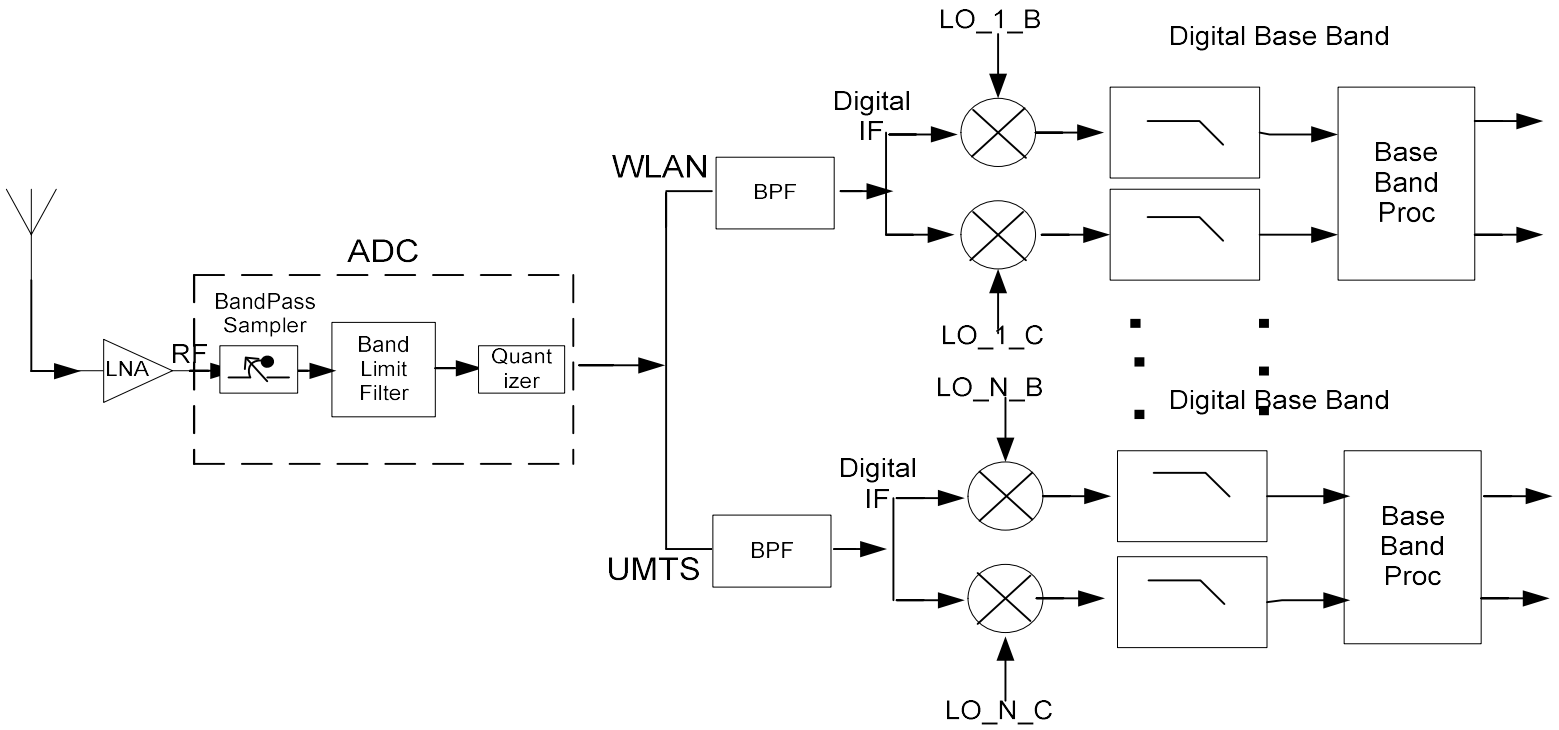
Outline

- Lecture 12: Software Defined Radio Architectures – Bandpass sampling
  - Brief Followup

- Lecture 12: SDR Cont…
  - Channelizer's design for SDR
    - Selection of Channelizer
    - Polyphase Cahnnelizer
    - Computational Complexity
  - Summary
  - Source: „*Digital Receivers and Transmitters Using Polyphase Filter Banks for Wireless Communications*“

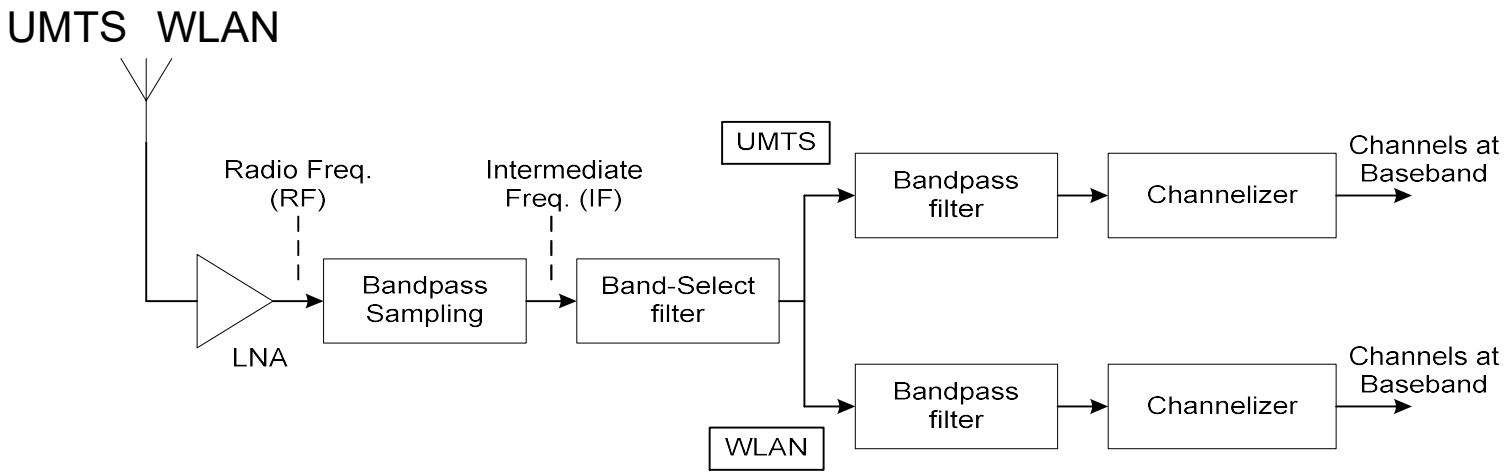
Proposed Software Radio Receiver Architecture

- Digital RF front end
- Digital IF (Decimation & Downconversion)

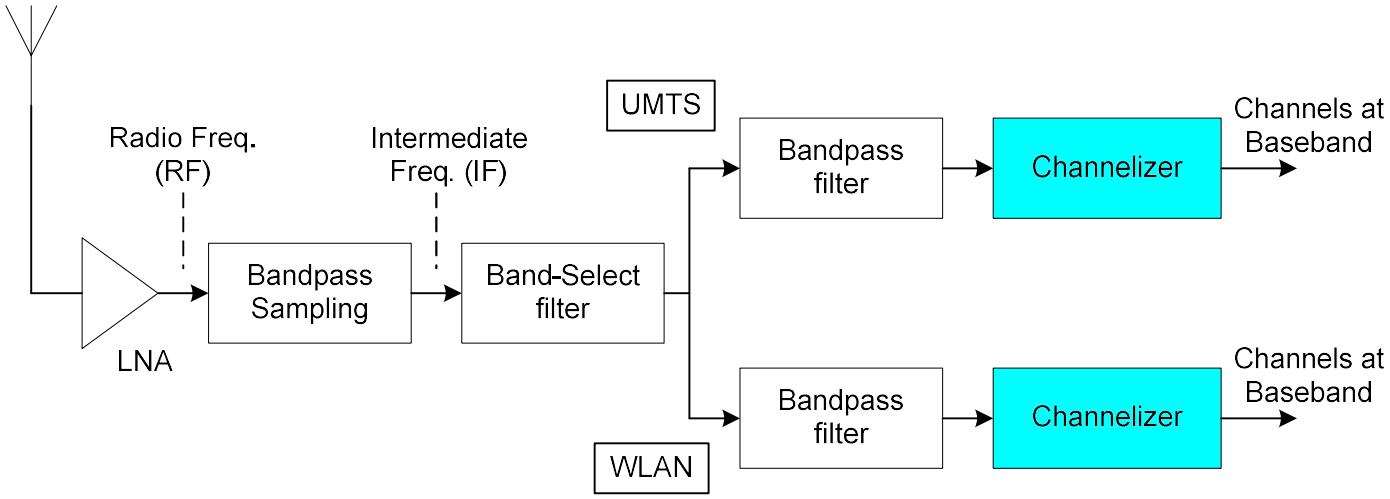


Multi-Standard Software Radio Receiver

System Block Diagram

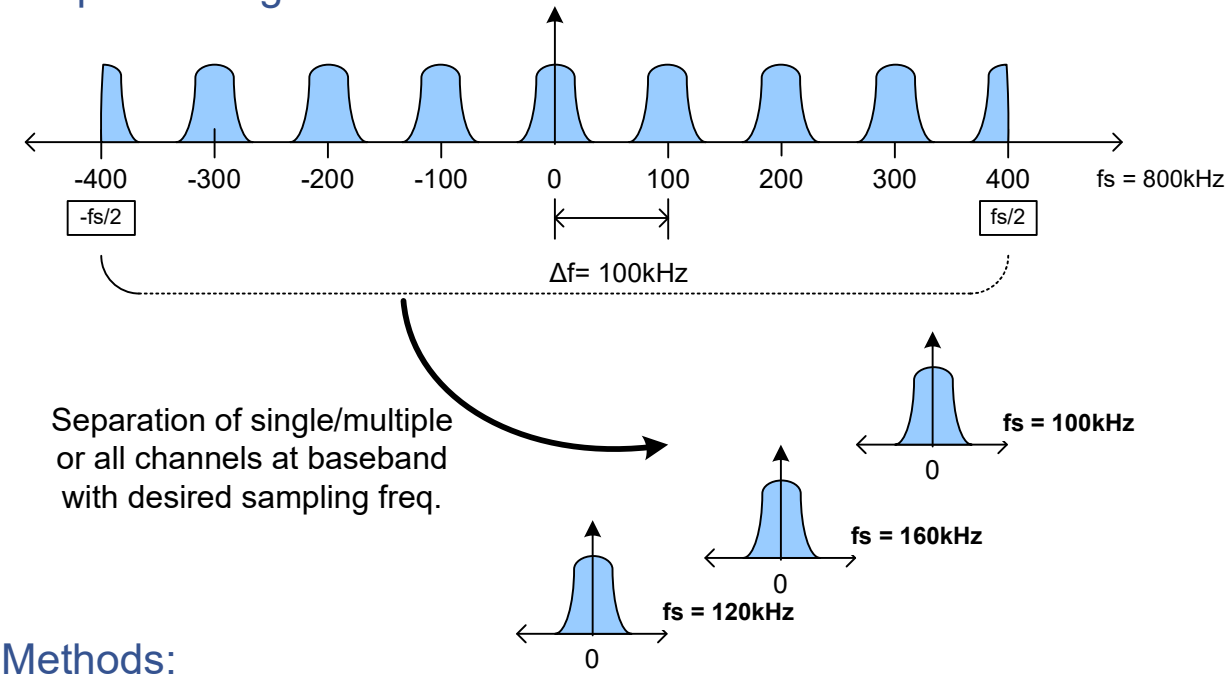


Channelizers



Channelization

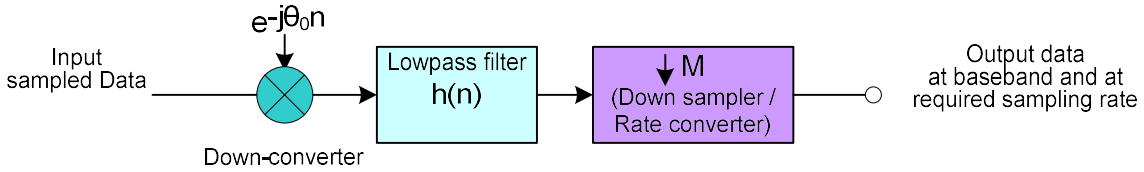
A process where a single, few or all channels from a certain frequency band are separated for further processing

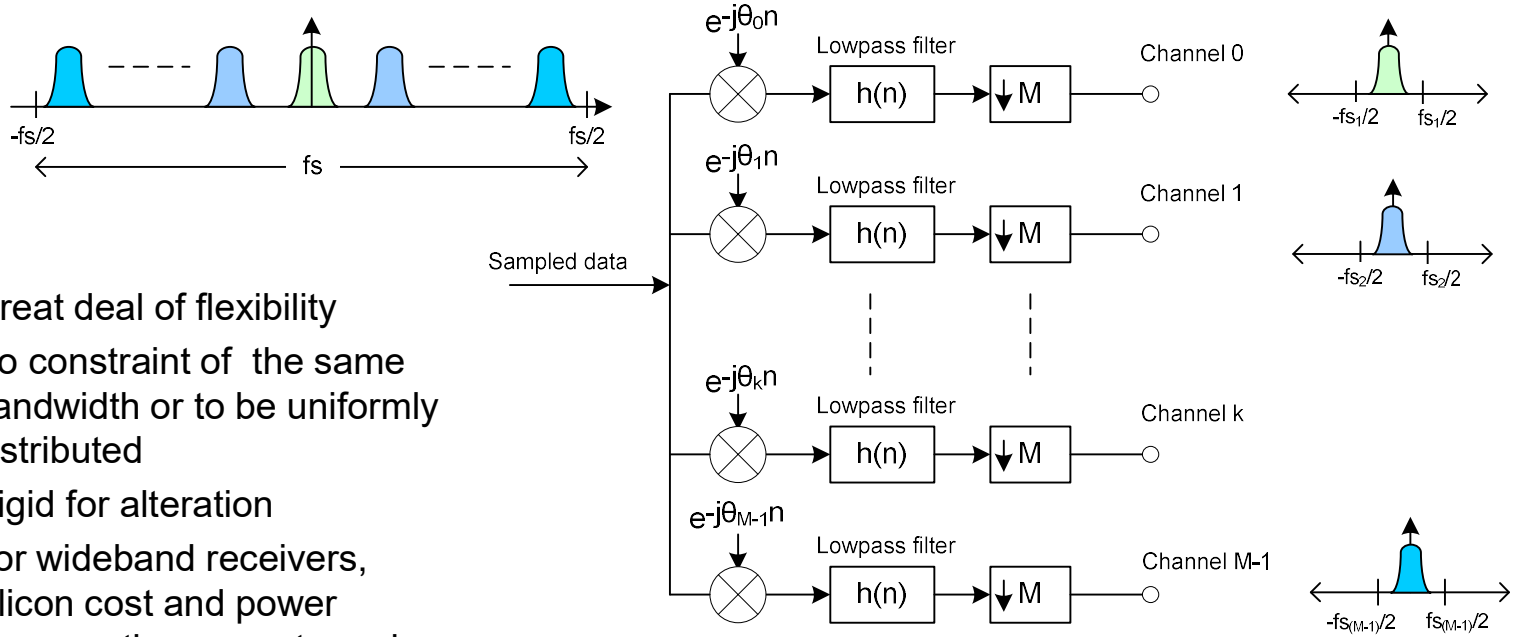


Channelization Methods:

- Per channel Approach (Straight forward way)
- Pipelined Frequency Transform
- Polyphase FFT

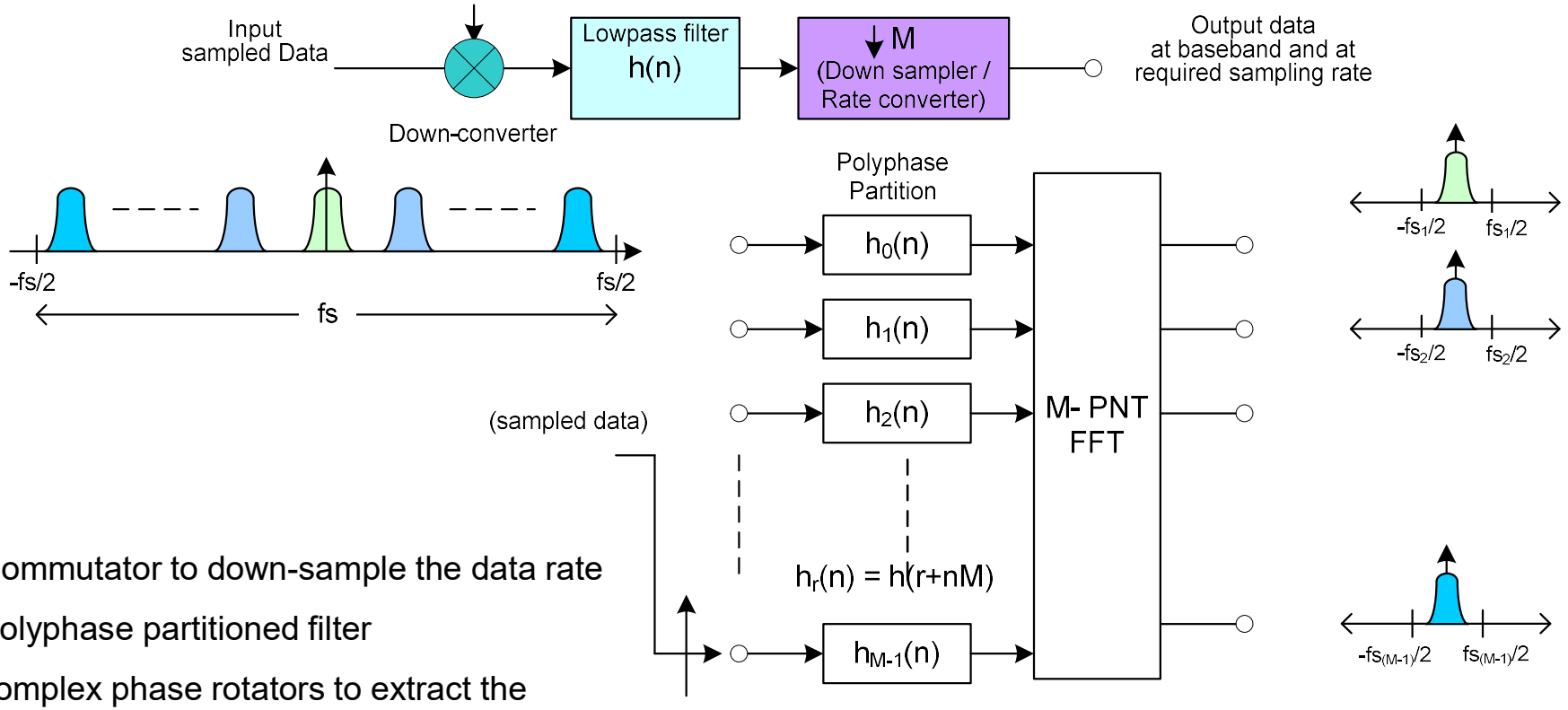
Per Channel Approach





- Great deal of flexibility
- No constraint of the same bandwidth or to be uniformly distributed
- Rigid for alteration
- For wideband receivers, silicon cost and power consumption are extremely high

Polyphase Channelizer



- Commutator to down-sample the data rate
- Polyphase partitioned filter
- complex phase rotators to extract the individaul channels
- Polyphase parameters
  - Input sampling frequency(fs)
    - Inter-carrier spacing (Δf)
    - Number of channels (M)

Pipelined Frequency Transform

- Based on binary tree of down-converter and sample-rate converter
- Divide the input band into two halves with half sampling rate
- Again split each half band into two sub-bands, and so on un-till the last tree level produces the required seperated channels
- More expensive in term of silicon area, because of many more single channel channelizer requirements
- Less flexible as it require channels to be equal bandwidth and uniformly distributed.

Comparison & Selection

Aspects		Channelizer Algorithms		
		Per Channel	Pipelined Frequency Transform	Polyphase FFT
Computational Complexity for high number of channels		Poor	Good	Excellent
Silicon Cost Efficiency		Upto 3-20 channels	Upto 128-256 channels	256 channels & above
Initial Design Flexibility	Independent Channels	Yes	No	No
	Number of Channels	selectable	2^{INT}	Preferable 2^{INT}
	Intermediate outputs	No	Yes	No
Flexibility for reconfiguration (Addition & Removal of Channels)		Excellent	Poor	poor

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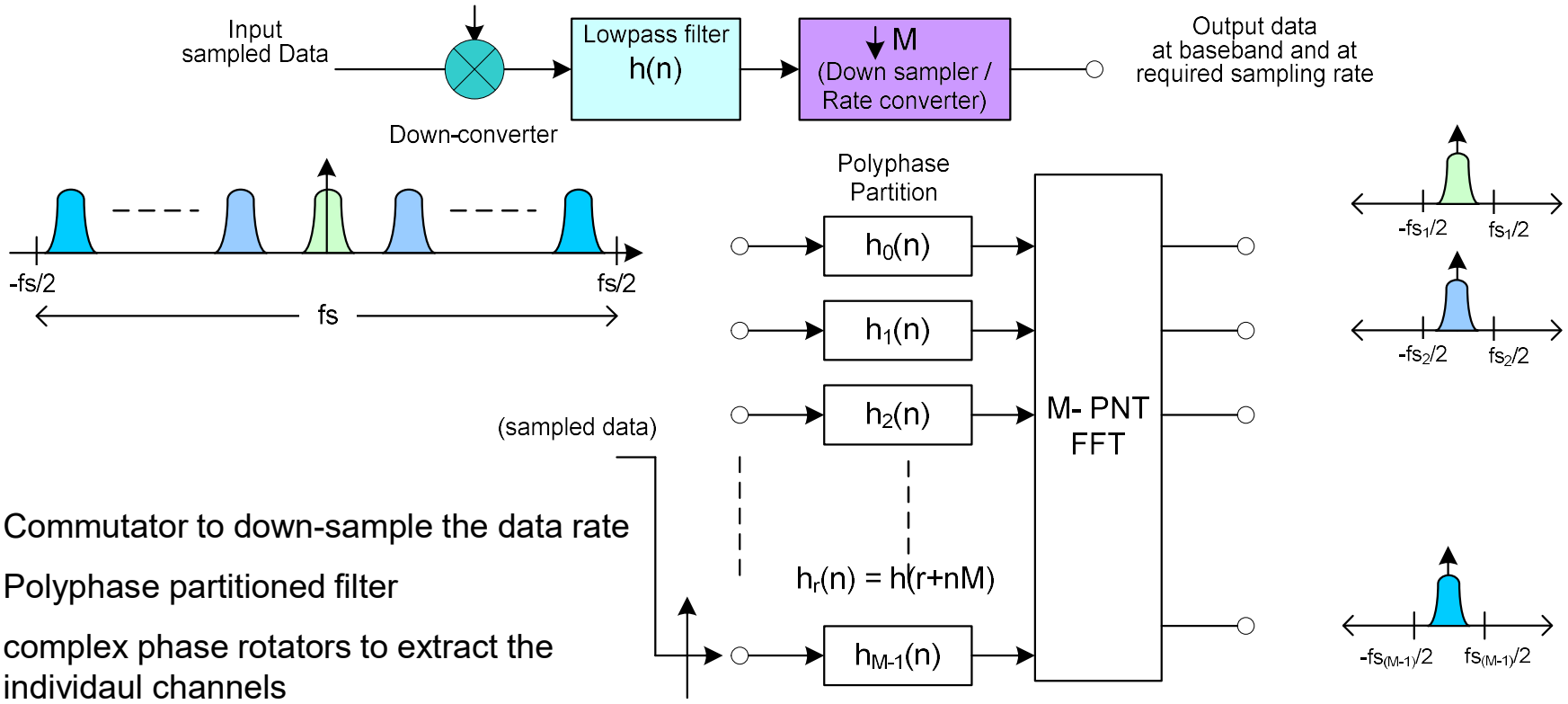
Per-channel approach wins in many aspects, but its implementation for high number of channels is infeasible

Polyphase channelizer is most suitable for SDR wideband channelizer front end

Polyphase Channelizer



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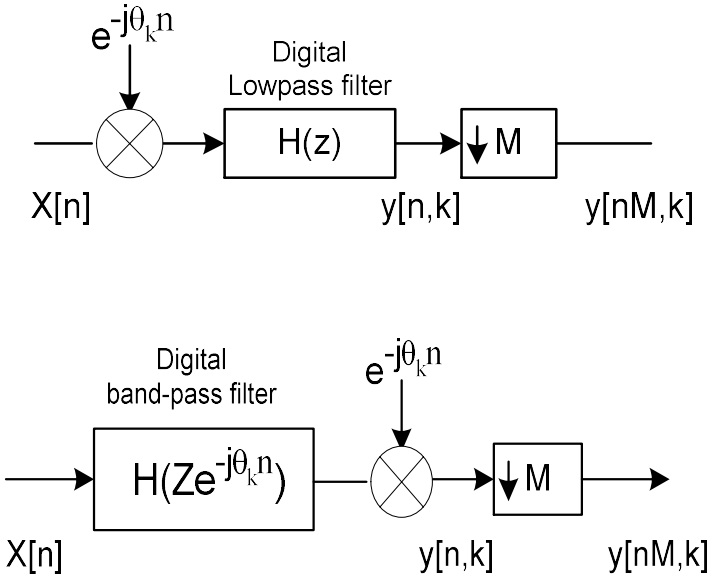
Polyphase Channelizer Transformation

Transformation (Step 1)

Equivalence Theorem:

”Operation of down-conversion, followed by a LPF are totally equivalent to the operation of BPF followed by a down conversion”



$$y(n,k) = [x(n)e^{-jn\theta_k}] * h(n)$$

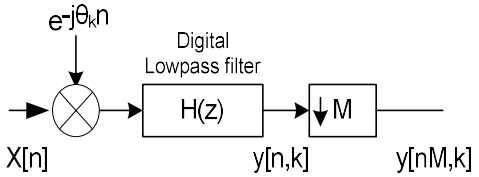
$$y(n,k) = \sum_{r=0}^{N-1} x[n-r]e^{-j\theta_k (n-r)} h(r)$$

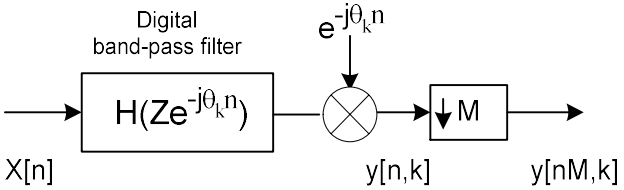
$$= \sum_{r=0}^{N-1} x[n-r]e^{-jn\theta_k} h(r)e^{jr\theta_k}$$

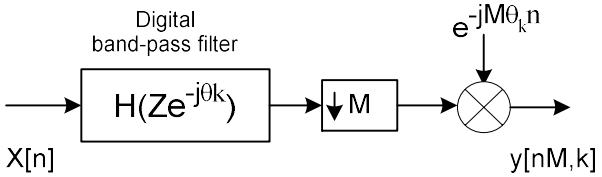
$$= e^{-jn\theta_k} \sum_{r=0}^{N-1} x[n-r]h(r)e^{jr\theta_k}$$

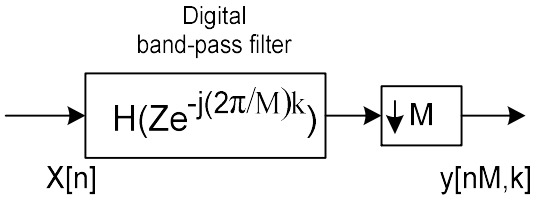
Equivalence Theorem & Sequence of maneuvers

- Slide the input heterodyne through the lowpass filter to their output
- By doing so, it converts the lowpass filter to a complex bandpass filter
- Slide the output heterodyne to the downside of the down-sampler
- Doing so, it aliases the centre frequency of the oscillator
- Restrict the centre frequency of bandpass to be a multiple of the output sample rate.
- Doing so, assure aliases of the selected passband to the baseband by re-sampling operation
- Discard the un-necessary heterodyne







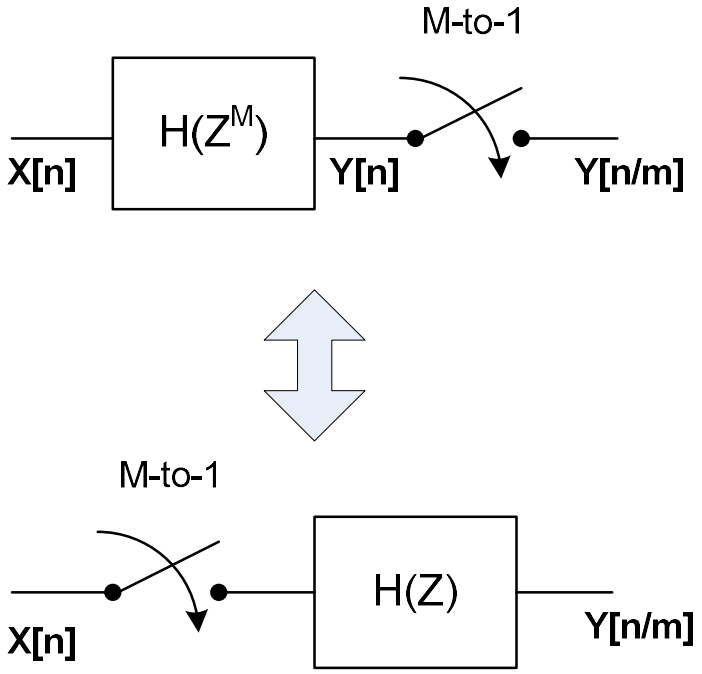


Note: θ_k should be an integer multiple of (2π/M)

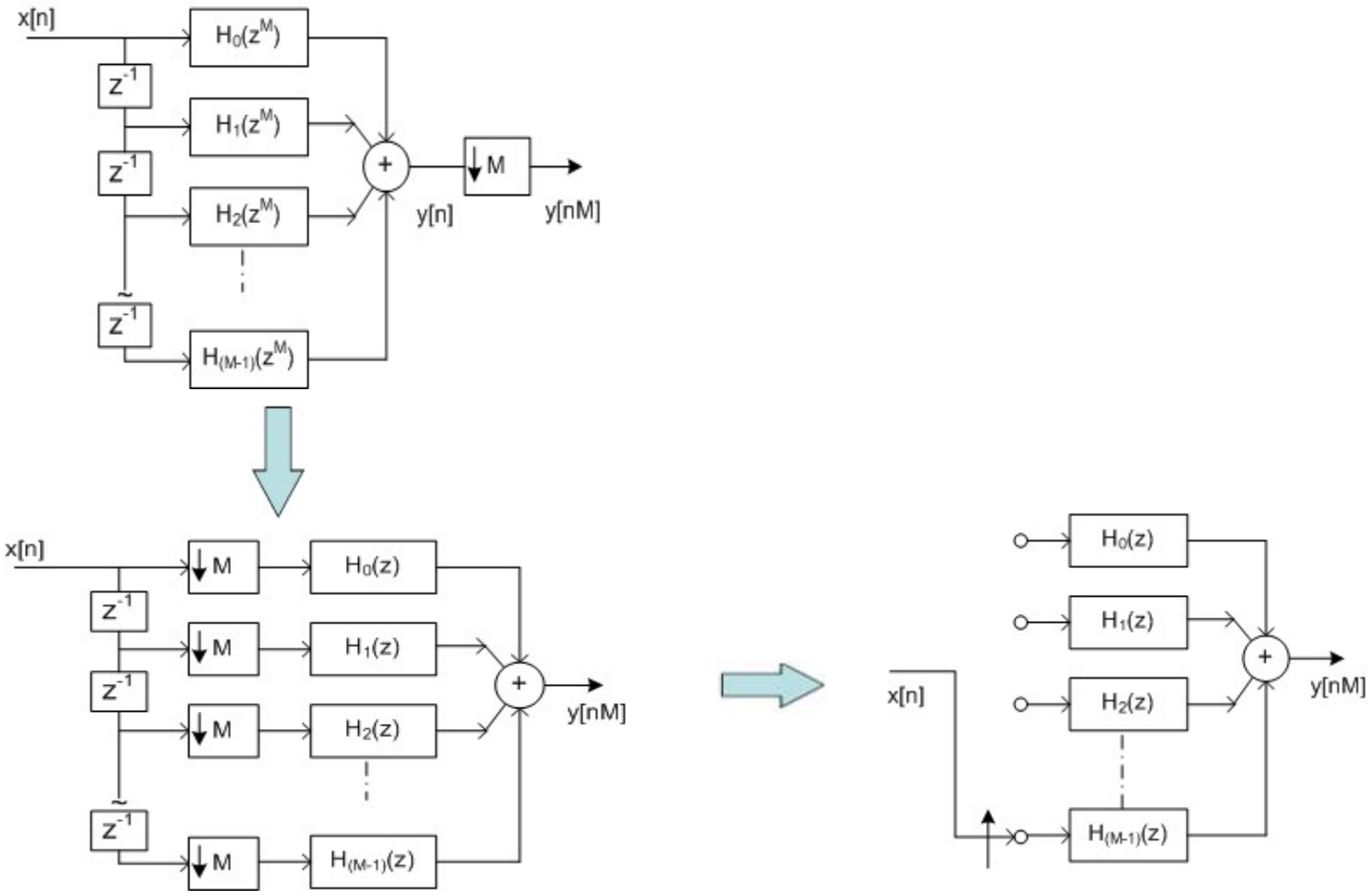
Transformation (Step 2)

Noble Identity:

” A filter processing every Mth input sample followed by an output M-to-1 down sampler is the same as an input M-to-1 down sampler followed by a filter processing every Mth input sample”



Transformation (Step 2)



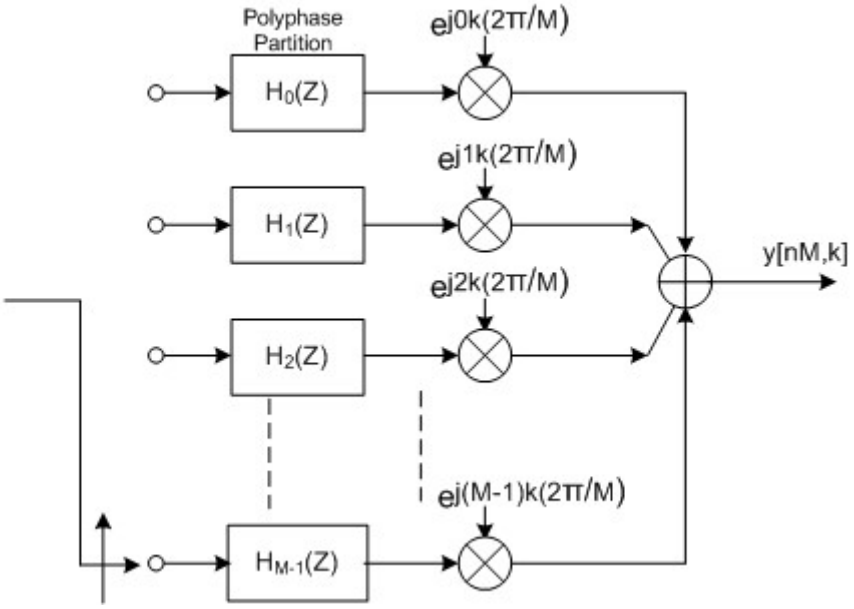
Transformation (Step 2)

$$H(z) = \sum_{n=0}^{N-1} Z^{-n} h(n)$$

$$G(z) = H(z)\big|_{z=e^{j\vartheta}z} = H(e^{-j\vartheta}z)$$

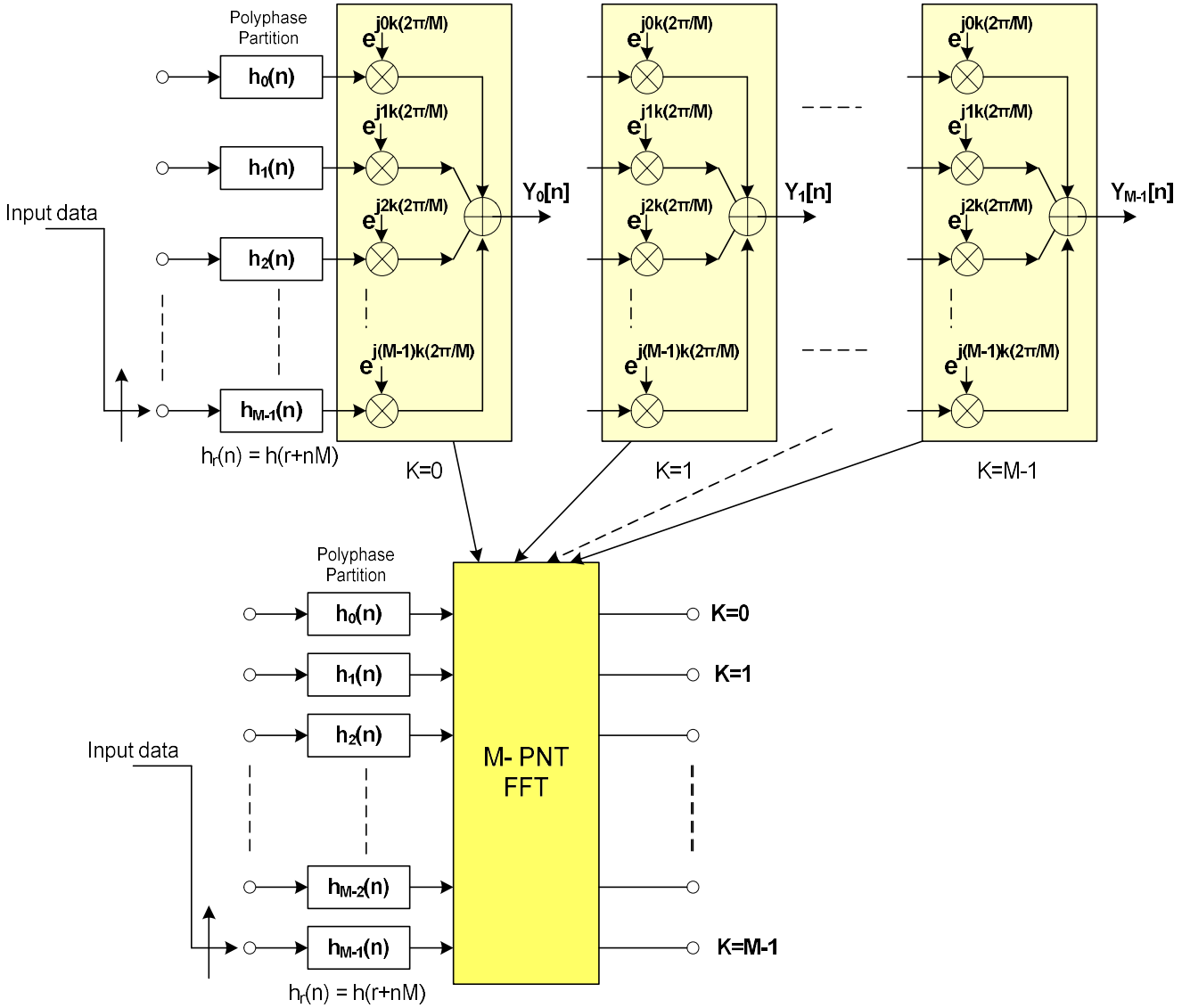
$$H(ze^{-j(2\pi/M)k}) = \sum_{r=0}^{M-1} Z^{-r} e^{j(2\pi/M)rk} H_r(z)$$

$$y(nM,k) = \sum_{r=0}^{M-1} y_r(nM) e^{j(2\pi/M)rk}$$

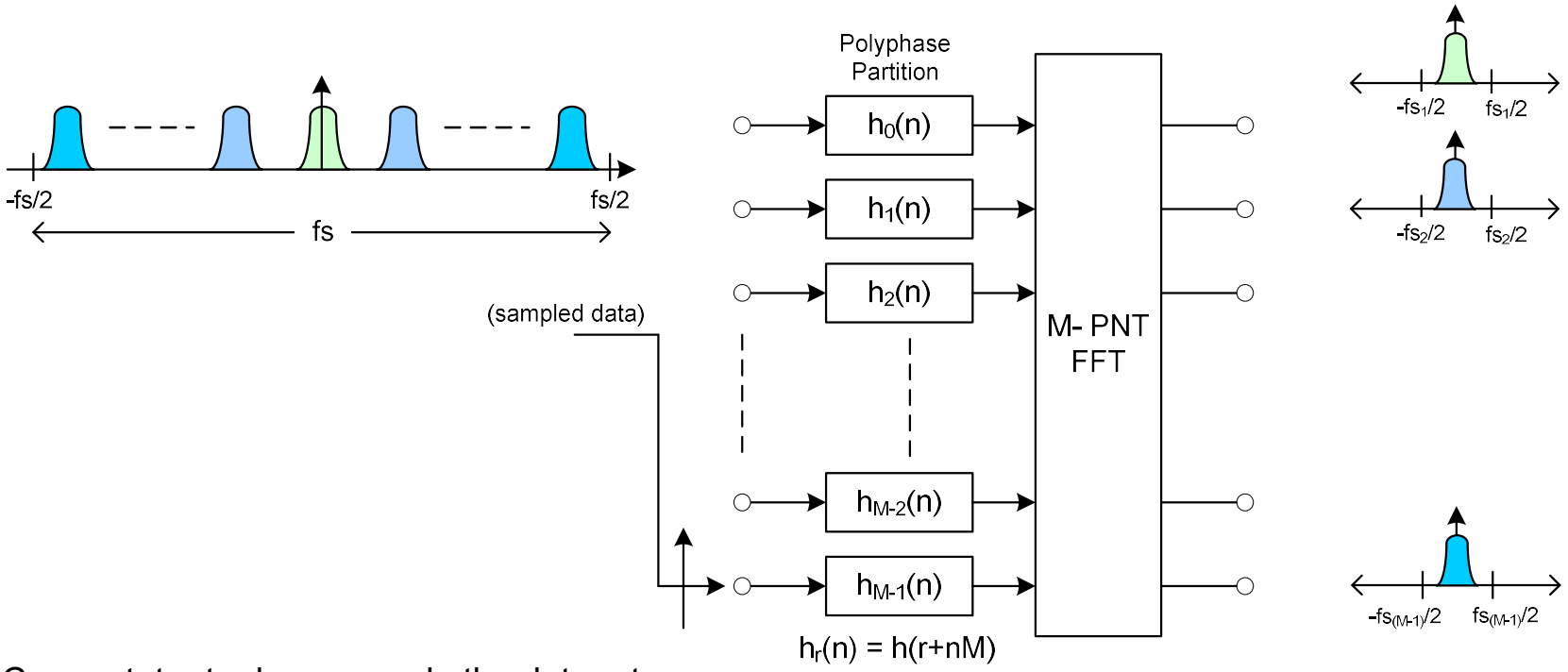


Re-sampling M-Path down converter

Phase Coherent summation & FFT



Polyphase Channelizer



- Commutator to down-sample the data rate
- Polyphase partitioned filter
- Complex phase rotators to extract the individual channels is equivalent to the M point FFT operation.

Polyphase filter bank parameters

Sampling Frequency, Number of Channels, Spectral Spacing, Output Sample Rate.

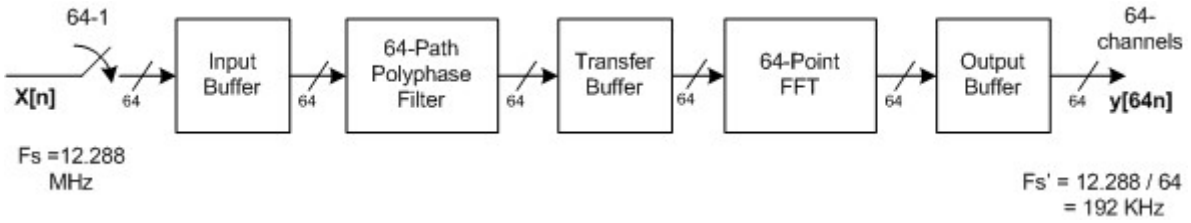
$$fs = N * \Delta f$$

- DFT performs the task of seperating the channels after polyphase filter, so it is natural to conclude that **transform size is equal to number of channels.**
- **The filter bandwidth is determined by the weights of the lowpass prototype filter, and it is common for all the channels.**
- Channelizer is used to seperate the adjacent communication channels, which are characterized by the **specifc center frequency and non-overlapping bandwidth**

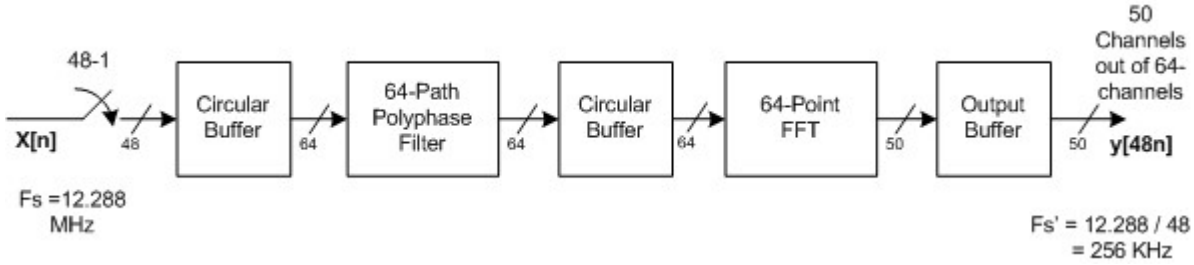
Maximally & Non-Maximally Decimated System

”A system is said to be Maximally Decimated when the ouput sample rate is equal to the inter-channel spacing otherwise it is non-maximally decimated system ”

Maximally Decimated



Non-Maximally Decimated



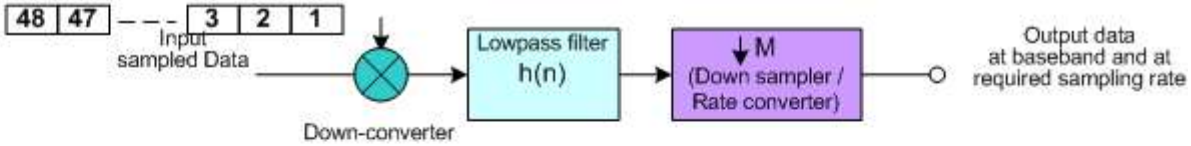
Computational Complexity

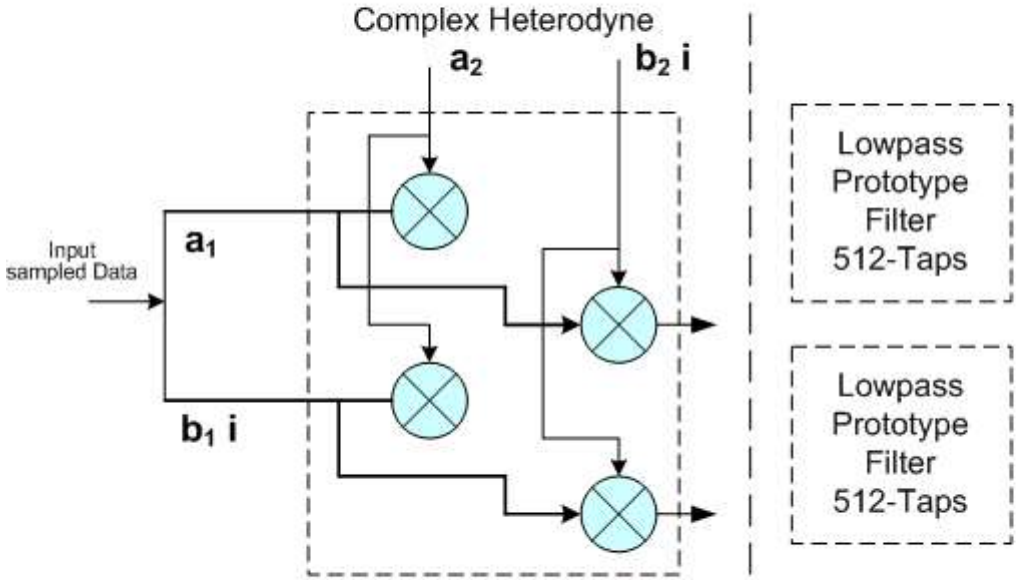
Work Load = Filter Length **/** Sample Ratio

= (no.of ops/output) **/ (**input/output)

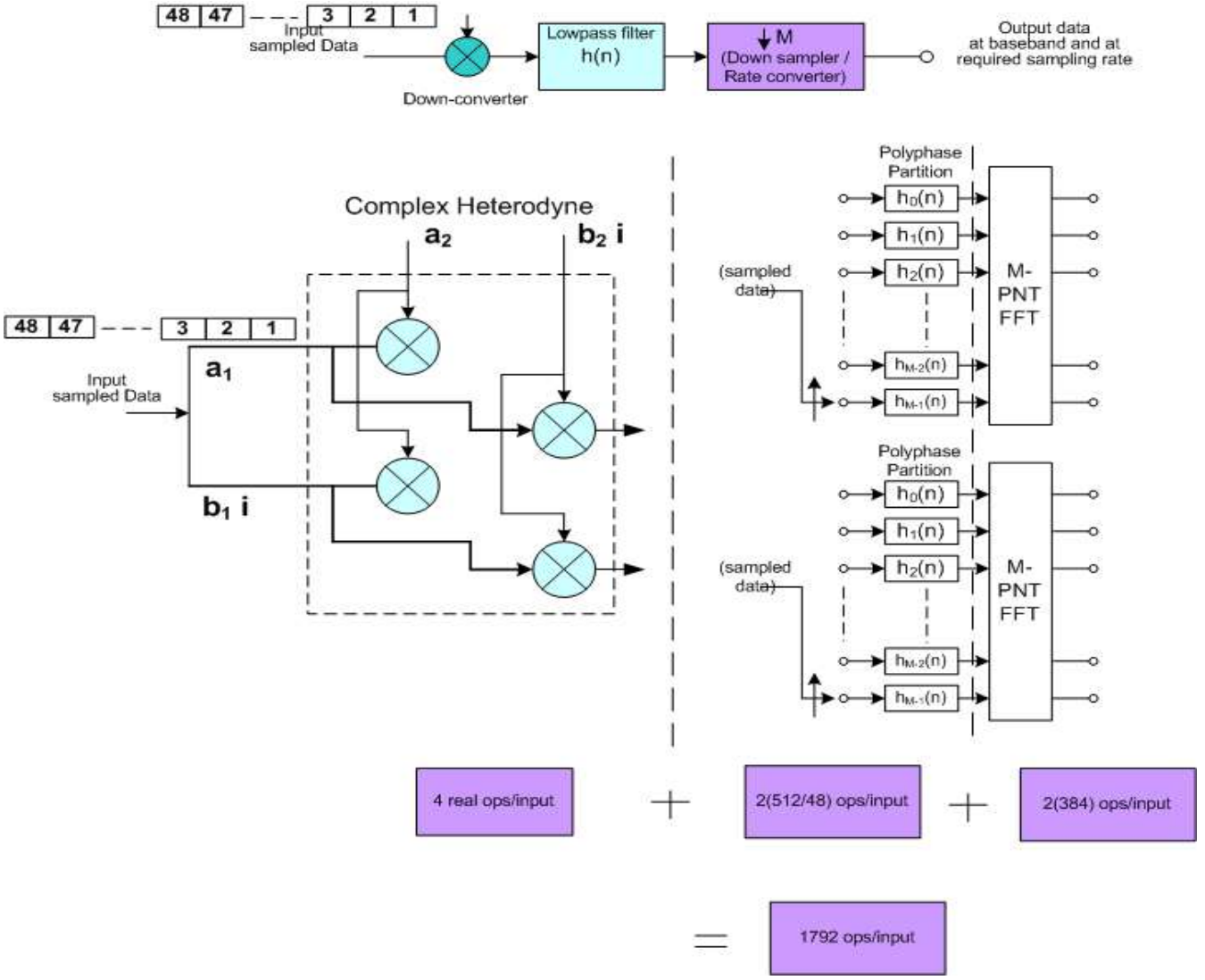
= no.of ops **/** input

Prototype Filter Work Load





Polyphase Filter Work Load



Computational Complexity

Does It make sense to use Polyphase filter for the Channelization ..... ???

Yes

Computational Complexity

1792 ops. **per 48 input**

work load = 1792/48 = 38 ops/input.

Note:

Polyphase channelizer forms 64 channels at the output and therefore, we conclude that polyphase form should be used even if just few output channels are required.

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Flexibility for reconfiguration (Addition & Removal of Channels)		Excellent	Poor	poor

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